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IS-IS protocol extensions for Path Computation Element (PCE) Discovery

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Abstract

There are various circumstances where it is highly desirable for a Path Computation Client (PCC) to be able to dynamically and automatically discover a set of Path Computation Element(s) (PCE), along with some of information that can be used for PCE selection. When the PCE is a Label Switch Router (LSR) participating to the IGP,

or even a server participating passively to the IGP, a simple and

efficient way for PCE discovery consists of relying on IGP flooding. For that purpose this document defines IS-IS extensions for the advertisement of PCE Discovery information within an IS-IS area or within the entire IS-IS routing domain.

Conventions used in this document

The key words "MUST", "MUST NOT", "REQUIRED", "SHALL", "SHALL NOT", "SHOULD", "SHOULD NOT", "RECOMMENDED", "MAY", and "OPTIONAL" in this document are to be interpreted as described in RFC-2119.

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1. Note (to be removed before publication)

This document specifies sub-TLVs to be carried within the IS-IS Router Capability TLV ([IS-IS-CAP]). Because this document does not introduce any new IS-IS element of procedure it will be discussed within the PCE Working Group with a review of the IS-IS Working Group.

2. Terminology

Terminology used in this document

ABR: IGP Area Border Router (L1L2 router).

AS: Autonomous System.

Domain: any collection of network elements within a common sphere of address management or path computational responsibility. Examples of domains include IGP areas and Autonomous Systems.

Intra-area TE LSP: A TE LSP whose path does not cross IGP area boundaries.

Intra-AS TE LSP: A TE LSP whose path does not cross AS boundaries.

Inter-area TE LSP: A TE LSP whose path transits through two or more IGP areas.

Inter-AS TE LSP: A TE LSP whose path transits through two or more ASes or sub-ASes (BGP confederations).

LSR: Label Switch Router.

PCC: Path Computation Client: any client application requesting a path computation to be performed by a Path Computation Element.

PCE: Path Computation Element: an entity (component, application, or network node) that is capable of computing a network path or route based on a network graph, and applying computational constraints.

PCEP: Path Computation Element communication Protocol.

TE LSP: Traffic Engineered Label Switched Path.

3. Introduction

[RFC4655] describes the motivations and architecture for a Path Computation Element (PCE)-based path computation model for Multi Protocol Label Switching (MPLS) and Generalized MPLS (GMPLS) Traffic Engineered Label Switched Paths (TE-LSPs). The model allows for the separation of PCE from PCC (also referred to as non co-located PCE) and allows for cooperation between PCEs. This relies on a communication protocol between PCC and PCE, and between PCEs. The requirements for such communication protocol can be found in [RFC4657] and the communication protocol is defined in [PCEP].

The PCE architecture requires, of course, that a PCC be aware of the location of one or more PCEs in its domain, and also potentially of some PCEs in other domains, e.g. in case of inter-domain TE LSP computation.

A network may comprise a large number of PCEs with potentially distinct capabilities. In such context it is highly desirable to have a mechanism for automatic and dynamic PCE discovery, which allows PCCs to automatically discover a set of PCEs, along with additional information required for PCE selection, and to dynamically detect new PCEs or any modification of PCE information. Detailed requirements for such a PCE discovery mechanism are described in [RFC4674].

Moreover, it may also be useful to discover when a PCE experiences some processing congestion state and exits such state, in order for the PCCs to take some appropriate actions (e.g. redirect to another PCE). Note that the PCE selection algorithm is out of the scope of this document.

When PCCs are LSRs participating to the IGP (OSPF, IS-IS), and PCEs are LSRs or a servers also participating to the IGP, an efficient mechanism for PCE discovery within an IGP routing domain consists of relying on IGP advertisements.

This document defines IS-IS extensions allowing a PCE participating to the IS-IS routing to advertise its location along with some information useful for PCE selection, so as to satisfy dynamic PCE discovery requirements set forth in [RFC4674]. This document also defines extensions allowing a PCE participating to the IS-IS routing to advertise its potential processing congestion state.

Generic capability mechanisms for IS-IS have been defined in [IS-IS-CAP] the purpose of which is to allow a router to advertise its capability within an IS-IS area or an entire IS-IS routing domain. Such IS-IS extensions fully satisfy the aforementioned dynamic PCE discovery requirements.

This document defines two new sub-TLVs (named the PCE Discovery (PCED) TLV and the PCE Status (PCES) TLV) for IS-IS, to be carried within the IS-IS Capability TLV ([IS-IS-CAP]). The PCE information

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advertised is detailed in section 4. Protocol extensions and procedures are defined in section 5 and 6.

This document does not define any new IS-IS element of procedure but how the procedures defined in [IS-IS-CAP] should be used.

The routing extensions defined in this document allow for PCE discovery within an IS-IS Routing domain. Solutions for PCE discovery across AS boundaries are beyond the scope of this document, and for further study.

This document defines a set of sub-TLVs that are nested within each other. When the degree of nesting TLVs is 2 (a TLV is carried within another TLV) the TLV carried within a TLV is called a sub-TLV. Strictly speaking, when the degree of nesting is 3, a subsub-TLV is

carried within a sub-TLV that is itself carried within a TLV. For the sake of terminology simplicity, we refer to sub-TLV, a TLV carried within a TLV regardless of the degree of nesting.

4. Overview

4.1. PCE Information

The PCE information advertised via IS-IS falls into two categories: PCE Discovery Information and PCE Status information.

4.1.1. PCE Discovery Information

The PCE Discovery information is comprised of:

- The PCE location: an IPv4 and/or IPv6 address that must be used to reach the PCE. It is RECOMMENDED to use addresses always reachable;

- The PCE inter-domain functions: PCE path computation scope (i.e. inter-area, inter-AS, inter-layer);

- The PCE domain(s): set of one or more domain(s) where the PCE has visibility and can compute paths;

- The PCE Destination domain(s): set of one or more destination domain(s) towards which a PCE can compute paths;

- A set of general PCEP capabilities (e.g. support for request prioritization) and path computation specific capabilities (e.g. supported constraints, supported objective functions).

Optional elements to describe more complex capabilities may also be advertised.

PCE Discovery information is by nature fairly static and does not change with PCE activity. Changes in PCE Discovery information may

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occur as a result of PCE configuration updates, PCE deployment/activation, PCE deactivation/suppression or PCE failure. Hence, this information is not expected to change frequently.

4.1.2. PCE Status Information

The PCE Status is optional and can be used to report a PCE processing congested state along with an estimated congestion duration. This is dynamic information, which may change with PCE activity.

Procedures for a PCE to move from a processing congested state to a non-congested state are beyond the scope of this document, but the rate at which a PCE Status change is advertised MUST not impact by any mean the IGP scalability. Particular attention should be given on procedures to avoid state oscillations.

4.2. Flooding scope

The flooding scope for PCE Discovery Information can be limited to one or more IS-IS areas the PCE belongs to or can be extended across the entire IS-IS routing domain.
Note that some PCEs may belong to multiple areas, in which case the flooding scope may comprise these areas. This could be the case of a L1L2 router for instance advertising its PCE information within the L2 level and/or a subset of its attached L1 area(s).

5. IS-IS extensions

5.1. IS-IS PCED TLV format

The IS-IS PCED TLV is made of various non ordered sub-TLVs.

The format of the IS-IS PCED TLV and its sub-TLVs is the same as the TLV format used by the Traffic Engineering Extensions to IS-IS [RFC3784]. That is, the TLV is composed of 1 octet for the type, 1 octet specifying the TLV length and a value field.

The IS-IS PCED TLV has the following format:

TYPE: To be assigned by IANA
LENGTH: Variable
VALUE: set of sub-TLVs

Sub-TLVs types are under IANA control.

Currently five sub-TLVs are defined (suggested type values to be assigned by IANA):

Sub-TLV type	Length	Name
1	variable	PCE-ADDRESS sub-TLV
2	3	PATH-SCOPE sub-TLV
3	variable	PCE-DOMAINS sub-TLV
4	variable	PCE-DEST-DOMAINS sub-TLV

5	variable	GENERAL-CAP sub-TLV
6	variable	PATH-COMP-CAP sub-TLV

The PCE-ADDRESS and PATH-SCOPE sub-TLVs MUST always be present within the PCED TLV.

The PCE-DOMAINS and PCE-DEST-DOMAINS sub-TLVs are optional. They may be present in the PCED TLV to facilitate selection of inter-domain PCEs.

The GENERAL-CAP and PATH-COMP-CAP sub-TLVs are optional and MAY be present in the PCED TLV to facilitate the PCE selection process.

Any non recognized sub-TLV MUST be silently ignored.

Additional sub-TLVs could be added in the future to advertise additional PCE information.

The PCED TLV is carried within an IS-IS CAPABILITY TLV defined in [IS-IS-CAP], whose S bit is determined by the desired flooding scope.

5.1.1. PCE-ADDRESS sub-TLV

The PCE-ADDRESS sub-TLV specifies the IP address that MUST be used to reach the PCE. It is RECOMMENDED to make use of an address that is always reachable, provided the PCE is alive.

The PCE-ADDRESS sub-TLV is mandatory; it MUST be present within the PCED TLV. It MAY appear twice, when the PCE has both an IPv4 and IPv6 address. It MUST NOT appear more than once for the same address type.

The PCE-ADDRESS sub-TLV has the following format:

TYPE: To be assigned by IANA (Suggested value =1)
LENGTH: 5 for IPv4 address and 17 for IPv6 address
VALUE: This comprises one octet indicating the address-type and 4 or 16 octets encoding the IPv4 or IPv6 address to be used to reach the PCE

Address-type:

1	IPv4
2	IPv6

5.1.2. The PATH-SCOPE sub-TLV

The PATH-SCOPE sub-TLV indicates the PCE path computation scope which refers to the PCE ability to compute or take part into the computation of intra-area, inter-area, inter-AS or inter-layer_TE LSP(s).

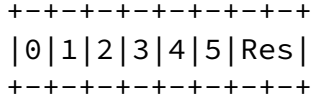
The PATH-SCOPE sub-TLV is mandatory; it MUST be present within the PCED TLV. There MUST be exactly one instance of the PATH-SCOPE sub-TLV within each PCED TLV.

The PATH-SCOPE sub-TLV contains a set of bit flags indicating the supported path scopes (intra-area, inter-area, inter-AS, inter-layer) and four fields indicating PCE preferences.

The PATH-SCOPE sub-TLV has the following format:

TYPE: To be assigned by IANA (Suggested value =2)
LENGTH: 3
VALUE: This comprises a one-byte flag of bits where each bit represents a supported path scope, followed by a 2-bytes preferences field indicating PCE preferences.

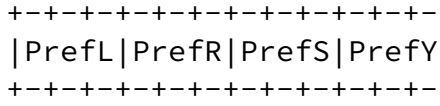
Here is the structure of the bits flag:



Bit	Path Scope
0	L bit: Can compute intra-area path
1	R bit: Can act as PCE for inter-area TE LSPs computation
2	Rd bit: Can act as a default PCE for inter-area TE LSPs computation
3	S bit: Can act as PCE for inter-AS TE LSPs computation
4	Sd bit: Can act as a default PCE for inter-AS TE LSPs

computation
5 Y bit: Can compute or take part into the computation of paths across layers
6-7 Reserved for future usage.

Here is the structure of the preferences field



Pref-L field: PCE's preference for intra-area TE LSPs computation.

Pref-R field: PCE's preference for inter-area TE LSPs computation.

Pref-S field: PCE's preference for inter-AS TE LSPs computation.

Pref-Y field: PCE's preference for inter-layer TE LSPs computation.

Res: Reserved for future usage.

The bits L, R, S and Y bits are set when the PCE can act as a PCE for intra-area, inter-area, inter-AS and inter-layer TE LSPs computation respectively. These bits are non mutually exclusive.

When set the Rd bit indicates that the PCE can act as a default PCE for inter-area TE LSPs computation (the PCE can compute path for any destination area). Similarly, when set the Sd bit indicates that the PCE can act as a default PCE for inter-AS TE LSPs computation (the PCE can compute path for any destination AS).

When the Rd bit is set, the PCE-DEST-DOMAIN TLV (see 5.1.4) does not contain any Area ID DOMAIN sub-TLV.

Similarly, when the Sd bit is set, the PCE-DEST-DOMAIN TLV does not contain any AS-DOMAIN sub-TLV.

The PrefL, PrefR, PrefS and PrefY fields are 3-bit long and allow the PCE to specify a preference for each computation scope, where 7 reflects the highest preference. Such preference can be used for

weighted load balancing of requests. An operator may decide to configure a preference to each PCE so as to balance the path computation load among them, with respect to their respective CPU capacity. The algorithms used by a PCC to balance its path computation requests according to such PCE's preference are out of the scope of this document. Same or distinct preferences may be used for different scopes. For instance an operator that wants a PCE capable of both inter-area and inter-AS computation to be used preferably for inter-AS computation may configure a PrefS higher than the PrefR. When the PrefL, PrefR, PRefS or PrefY is cleared, this indicates an absence of preference.

When the L bit, R bit, S or Y bit are cleared the PrefL, PrefR, PrefS, PrefY fields MUST respectively be set to 0.

5.1.3. PCE-DOMAINS sub-TLV

The PCE-DOMAINS sub-TLV specifies the set of domains (areas or AS) where the PCE has topology visibility and can compute paths. It contains a set of one or more sub-TLVs where each sub-TLV identifies a domain.

The PCE-DOMAINS sub-TLV MUST be present when PCE domains cannot be inferred by other IGP information, for instance when the PCE is inter-domain capable (i.e. when the R bit or S bit is set) and the flooding scope is the entire routing domain.

The PCE-DOMAINS sub-TLV has the following format:

TYPE: To be assigned by IANA (Suggested value =2)
LENGTH: Variable
VALUE: This comprises a set of one or more DOMAIN sub-TLVs where each DOMAIN sub-TLV identifies a domain where the PCE has topology visibility and can compute paths

DOMAIN sub-TLVs types are under IANA control.

Currently two DOMAIN sub-TLVs are defined (suggested type values to be assigned by IANA):

Sub-TLV type	Length	Name
1	variable	Area ID sub-TLV
2	4	AS number sub-TLV

At least one DOMAIN sub-TLV MUST be present in the PCE-DOMAINS sub-TLV. Note than when the PCE visibility is an entire AS, the PCE-DOMAINS sub-TLV MUST uniquely include one AS number sub-TLV.

5.1.3.1. Area ID DOMAIN sub-TLV

This sub-TLV carries an IS-IS area ID. It has the following format

TYPE: To be assigned by IANA (Suggested value =1)
LENGTH: Variable
VALUE: This comprises a variable length IS-IS area ID. This is the combination of an Initial Domain Part (IDP) and High Order part of the Domain Specific part (HO-DSP)

5.1.3.2. AS Number DOMAIN sub-TLV

The AS Number sub-TLV carries an AS number. It has the following format:

TYPE: To be assigned by IANA (Suggested value =2)
LENGTH: 4
VALUE: AS number identifying an AS. When coded on two bytes (which is the current defined format as the

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time of writing this document), the AS Number field MUST have its left two bytes set to 0.

5.1.4. PCE-DEST-DOMAINS sub-TLV

The PCE-DEST-DOMAINS sub-TLV specifies the set of destination domains (areas, AS) toward which a PCE can compute paths. It means that the PCE can compute or take part in the computation of inter-domain TE LSPs whose destinations are located within one of these domains. It contains a set of one or more DOMAIN sub-TLVs where each DOMAIN sub-

TLV identifies a domain.

The PCE-DEST-DOMAINS sub-TLV has the following format:

TYPE: To be assigned by IANA (Suggested value =3)
LENGTH: Variable
VALUE: This comprises a set of one or more area or/and AS DOMAIN sub-TLVs where each sub-TLV identifies a destination domain toward which a PCE can compute path.

The PCE-DEST-DOMAINS sub-TLV MUST be present if the R bit is set and the Rd bit is cleared, and/or, if the S bit is set and the Sd bit is cleared.

The PCE-DEST-DOMAINS sub-TLV MUST include at least one DOMAIN sub-TLV. It MUST include at least one area ID sub-TLV, if the R bit of the PATH-SCOPE TLV is set and the Rd bit of the PATH-SCOPE TLV is cleared. Similarly, it MUST include at least one AS number sub-TLV if the S bit of the PATH-SCOPE TLV is set and the Sd bit of the PATH-SCOPE TLV is cleared.

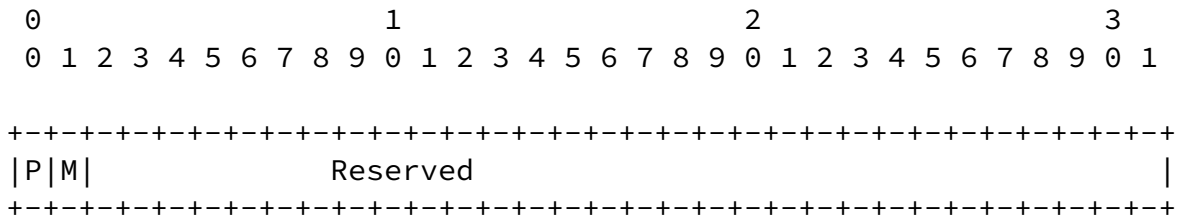
5.1.5. GENERAL-CAP sub-TLV

The GENERAL-CAP sub-TLV is an optional TLV used to indicate PCEP related capabilities. It carries a 32-bit flag, where each bit corresponds to a general PCE capability. It MAY also include optional sub-TLVs to encode more complex capabilities.

The GENERAL-CAP sub-TLV has the following format:

TYPE: To be assigned by IANA (Suggested value =4)
LENGTH: Variable
VALUE: This comprises a 32-bit General Capabilities flag where each bit corresponds to a general PCE capability, and optional sub-TLVs that may be defined to specify more complex capabilities. Currently no sub-TLVs are defined.

The following bits in the General Capabilities 32-bit flag are to be assigned by IANA:



Bit	Capabilities
0	P bit: Support for Request prioritization.
1	M bit: Support for multiple requests within the same request message.
2-31	Reserved for future assignments by IANA.

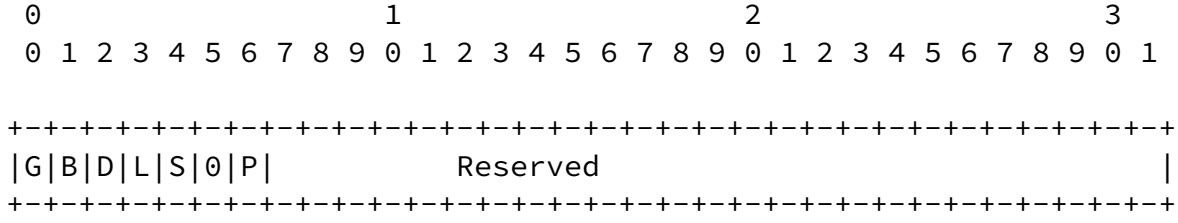
5.1.6. The PATH-COMP-CAP sub-TLV

The PATH-COMP-CAP sub-TLV is an optional TLV used to indicate path computation specific capabilities of a PCE.
It comprises a 32-bit flag, where each bit corresponds to a path computation capability. It MAY also include optional sub-TLVs to encode more complex capabilities.

The PATH-COMP-CAP sub-TLV has the following format:

TYPE: To be assigned by IANA (suggested value = 5)
LENGTH: Variable
VALUE: This comprises one 32 bit Path Computation Capabilities Flag, where each bit corresponds to a path computation capability, and optional sub-TLVs that may be defined to specify more complex capabilities. Three optional sub-TLVs are currently defined.

The following bits in the Path Computation Capabilities 32-bit Flag are to be assigned by IANA:



Bit	Capabilities
0	G bit: Capability to handle GMPLS link contraints

1	B bit: Capability to compute bidirectional paths
2	D bit: Capability to compute link/node/SRLG diverse paths
3	L bit: Capability to compute load-balanced paths
4	S bit: Capability to compute a set of paths in a synchronized Manner
5	O bit: Support for multiple objective functions
6	P bit: Capability to handle path constraints (e.g. max hop count, metric bound)
7-31	Reserved for future assignments by IANA.

The G, B, D, L, S, O and P bits are not exclusive.

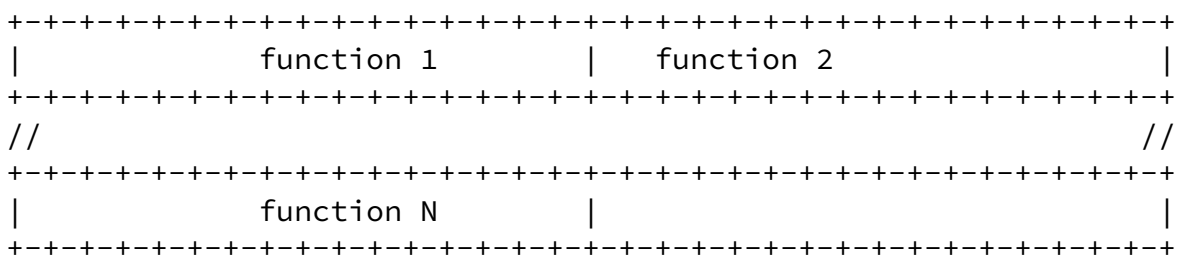
Three optional sub-TLVs are currently defined for the PATH-COMP-CAP TLV:

- The Objective Functions sub-TLV (type to be defined, suggested value =1) that carries a list of supported objective functions, where each objective function is identified by a 16 bit integer.
- The Opaque Objective Function sub-TLV (type to be defined, suggested value =2) that allows the user to encode a specific objective function in any appropriate language.
- The Switch Caps sub-TLV (type to be defined, suggested value =3) that carries a list of supported switching capabilities. This means that the PCE can compute paths for the listed switching capabilities.

5.1.6.1. Objective Functions sub-TLV

The format of the Objective Functions sub-TLV is as follows:

TYPE:	To be defined by IANA (suggested value =1)
LENGTH:	Variable (N*2)
VALUE:	This comprises a set of one or more 16 bit function ids, where each function id identifies a supported objective functions.



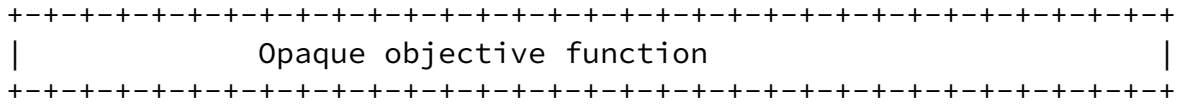
Objectives functions and their identification will be defined in a separate document.

The Objective Functions sub-TLV is optional. It MAY be present within the PATH-COMP-CAP TLV. When present it MUST be present only once in the PATH-COMP-CAP TLV.

5.1.6.2. Opaque Objective Function sub-TLV

The format of the Opaque Objective Function sub-TLV is as follows:

```
TYPE:     To be defined by IANA (suggested value =2)
LENGTH:   Variable
VALUE:    This encodes a specific objective function in any
          appropriate language.
```

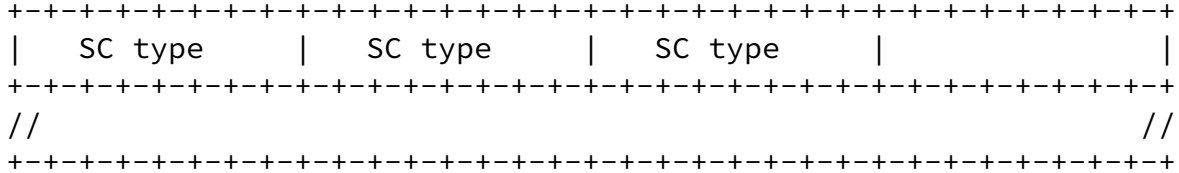


The Opaque Objective function sub-TLV is optional. The PATH-COMP-CAP TLV MAY comprise 0, one or more Opaque Objective Functions.

5.1.6.3. Switch Caps sub-TLV

The format of the Switch Caps sub-TLV is as follows:

```
TYPE     To be defined by IANA (suggested value =3)
LENGTH   Variable = N, where N is the number of supported
         switching capabilities
VALUE    This comprises a set of one or more 8-bit switching
         types, where each switching types identifies a
         supported switching capability.
```



Switching type values are defined in [RFC4205].

The Switch Caps sub-TLV is optional. It MAY be present in the PATH-COMP-CAP TLV. When present it MUST be present only once in the PATH-COMP-CAP

TLV.

5.2. The IS-IS PCES sub-TLV

The IS-IS PCE Status TLV (PCES sub-TLV) carries information related to PCE processing congestion state. The PCES sub-TLV is carried within an IS-IS Capability TLV which is defined in [IS-IS-CAP].

The IS-IS PCES sub-TLV has the following format:

TYPE: To be assigned by IANA
LENGTH: Variable
VALUE: set of sub-TLVs

Sub-TLVs types are under IANA control.

Currently two sub-TLVs are defined (suggested type values to be assigned by IANA):

Sub-TLV type	Length	Name
1	variable	PCE-ADDRESS sub-TLV
2	3	CONGESTION sub-TLV

There MUST be exactly one occurrence of the PCE-ADDRESS and CONGESTION sub-TLVs within a PCES sub-TLV. The PCE-ADDRESS sub-TLV is defined in section 5.1.1. It carries one of the PCE IP addresses and is used to identify the PCE experiencing a processing congestion state. This is required as the PCES and PCED TLVs may be carried in separate IS-IS Capability TLVs.
A PCE implementation MUST use the same IP address for the PCE-ADDRESS sub-TLV carried within the PCED sub-TLV and the PCE-ADDRESS sub-TLV carried within the PCES sub-TLV.

Any non recognized sub-TLV MUST be silently ignored.

Additional sub-TLVs could be added in the future to advertise additional congestion information.

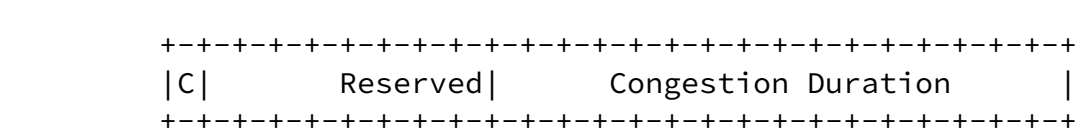
5.2.1. The CONGESTION sub-TLV

The CONGESTION sub-TLV is used to indicate whether a PCE experiences a processing congestion state or not along with optionally the PCE expected congestion duration.
The CONGESTION sub-TLV is mandatory. There MUST be a single instance of the CONGESTION sub-TLV within the PCES TLV.

The format of the CONGESTION sub-TLV is as follows:

TYPE: To be assigned by IANA (Suggested value =2)
LENGTH: 3
VALUE: This comprises a one-byte flag of bits indicating the congestion status, followed by a 2-bytes field indicating the congestion duration.

Here is the TLV structure



Value
-C bit: When set this indicates that the PCE experiences congestion and cannot accept any new request. When cleared this indicates that the PCE does not experience congestion and can accept new requests.

-Congestion Duration: 2-bytes, the estimated PCE congestion duration in seconds.

When C is set and the Congestion Duration field is equal to 0, this means that the Congestion Duration is unknown.
When C is cleared the Congestion Duration MUST be set to 0.

6. Elements of Procedure

The PCED and PCES TLV are carried within an IS-IS Capability TLV defined in [IS-IS-CAP].

As PCES information is likely to change more frequently than the PCED information, it is RECOMMENDED to carry PCES and PCED TLVs in separate IS-IS Capability TLVs, so as not to carry all PCED information each time the PCE status changes.

An IS-IS router MUST originate a new IS-IS LSP whenever the content of any of the PCED TLV or PCES TLV changes or whenever required by the regular IS-IS procedure (LSP refresh).

When the scope of the PCED or PCES TLV is area local it MUST be carried within an IS-IS CAPABILITY TLV having the S bit cleared. When the scope of the PCED or PCES TLV is the entire IGP domain, the PCED TLV MUST be carried within an IS-IS CAPABILITY TLV having the S bit set.
When only the L bit of the PATH-SCOPE sub-TLV is set, the flooding scope MUST be local.
Note that the flooding scopes of the PCED and PCES TLVs may be distinct, in which case they are carried in distinct IS-IS Capability TLVs.

The PCED and PCES sub-TLVs are OPTIONAL. When an IS-IS LSP does not contain any PCED or PCES sub-TLV, this means that the PCE information of that node is unknown.

A change in PCED or PCES information MUST not trigger any SPF computation.

The way PCEs retrieve their own information is out of the scope of this document. Some information may be configured (e.g. address, preferences, scope) and other information may be automatically retrieved (e.g. areas of visibility).

6.1.1. PCES TLV specific procedure

When a PCE enters into a processing congestion state, the conditions of which are implementation dependent, it SHOULD originate a new IS-IS LSP with a Capability TLV carrying a PCES TLV with the C bit set

and optionally a non-null expected congestion duration.

When a PCE exists from the processing congestion state, the conditions of which are implementation dependent, two cases are considered:

- If the congestion duration in the previously originated PCES TLV was null, it SHOULD originate a PCES TLV with the C bit cleared and a null congestion duration;
- If the congestion duration in the previously originated PCES TLV was non null, it MAY originate a PCES TLV. Note that in some particular cases it may be desired to originate a PCES TLV with the C bit cleared if the congestion duration was over estimated.

The congestion duration allows reducing the amount of IS-IS flooding, as only uncongested-to-congested state transitions are advertised.

An implementation SHOULD support an appropriate dampening algorithm so as to dampen IS-IS flooding in order to not impact the IS-IS scalability. It is RECOMMENDED to introduce some hysteresis for congestion state transition, so as to avoid state oscillations that may impact IS-IS performances. For instance two thresholds MAY be configured: a resource congestion upper-threshold and a resource congestion lower-threshold. An LSR enters the congested state when the CPU load reaches the upper threshold and leaves the congested state when the CPU load goes under the lower threshold.

Upon receipt of an updated PCES TLV a PCC should take appropriate actions. In particular, the PCC SHOULD stop sending requests to a congested PCE, and SHOULD gradually start sending again requests to a no longer congested PCE.

7. Backward compatibility

The PCED and PCES TLVs defined in this document do not introduce any interoperability issue.
An IS-IS router not supporting the PCED/PCES TLVs will just silently ignore the TLV as specified in [IS-IS-CAP].

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8. IANA considerations

8.1. IS-IS sub-TLVs

IANA will assign two new codepoints for the PCED and PCES sub-TLVs carried within the IS-IS CAPABILITY TLV defined in [IS-IS-CAP].

Type	Description	Reference
1	PCED	[IS-IS-CAP]
2	PCES	[IS-IS-CAP]

8.1.1 Sub-TLVs of the PCED sub-TLV

IANA is requested to manage sub-TLV types for the PCED sub-TLV.

Five sub-TLVs types are defined for the PCED sub-TLV and should be assigned by IANA:

Type	Description	Reference
1	PCE-ADDRESS	This document
2	PATH-SCOPE	This document
3	PCE-DOMAINS	This document
4	PCE-DEST-DOMAINS	This document
5	GENERAL-CAP	This document
6	PATH-COMP-CAP	This document

Sub-TLVs of the PCE-DOMAINS and and PCE-DEST-DOMAINS sub-TLVs

Two sub-TLVs types are defined for the PCE-DOMAINS and PCE-DEST-DOMAINS sub-TLVs and should be assigned by IANA:

Type	Description	Reference
1	Area ID	This document
2	AS Number	This document

Sub-TLV of the PATH-COMP-CAP sub-TLV

Three sub-TLV types are defined for the PATH-COMP-CAP sub-TLV and should be assigned by IANA:

Type	Description	Reference
1	Objective Functions	This document
2	Opaque Objective Function	This document
3	Switch Caps sub-TLV	This document

8.1.2 Sub-TLVs of the PCES sub-TLV

IANA is requested to manage sub-TLV types for the PCES TLV.

Type	Description	Reference
1	PCE-ADDRESS	This document
2	CONGESTION	This document

8.2. Capability bits

IANA is requested to manage the space of the General Capabilities 32-bit flag and the Path Computation Capabilities 32-bit flag defined in this document, numbering them in the usual IETF notation starting at zero and continuing through 31.
New bit numbers may be allocated only by an IETF Consensus action.
Each bit should be tracked with the following qualities:

- Bit number
- Defining RFC
- Name of bit

Currently two bits are defined in the General Capabilities flag. Here are the suggested values:

-0: Support for Request prioritization.
-1: Support for multiple messages within the same request message

Currently seven bits are defined in the Path Computation Capabilities flag. Here are the suggested values:

-0: Capability to handle GMPLS Constraints
-1: Capability to compute bidirectional paths
-2: Capability to compute link/node/SRLG diverse paths
-3: Capability to compute load-balanced paths
-4: Capability to compute a set of paths in a synchronized Manner
-5: Support for multiple objective function
-6: Capability to handle path constraints (e.g. hop count, metric bound)

9. Security Considerations

Any new security issues raised by the procedures in this document depend upon the opportunity for LSPs to be snooped, the ease/difficulty of which has not been altered. As the LSPs may now contain additional information regarding PCE capabilities, this new information would also become available. Mechanisms defined to

secure ISIS Link State PDUs [RFC3567], and their TLVs, can be used to secure PCED and PCES TLVs as well.

10. Manageability Considerations

Manageability considerations for PCE Discovery are addressed in section 4.10 of [RFC4674].

11. Acknowledgments

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12. References

12.1. Normative references

[RFC2119] Bradner, S., "Key words for use in RFCs to Indicate Requirement Levels", BCP 14, RFC 2119, March 1997.

[RFC3667] Bradner, S., "IETF Rights in Contributions", BCP 78, RFC 3667, February 2004.

[BCP79] Bradner, S., "Intellectual Property Rights in IETF Technology", RFC 3979, March 2005.

[IS-IS] "Intermediate System to Intermediate System Intra-Domain Routing Exchange Protocol " ISO 10589.

[RFC1195] Callon, R., "Use of OSI IS-IS for routing in TCP/IP and dual environments", RFC 1195, December 1990.

[RFC3784] Li, T., Smit, H., "IS-IS extensions for Traffic Engineering", RFC 3784, June 2004.

[IS-IS-CAP] Vasseur, J.P. et al., "IS-IS extensions for advertising router information", draft-ietf-isis-caps, work in progress.

[RFC4655] Farrel, A., Vasseur, J.P., Ash, J., "Path Computation Element (PCE)-based Architecture", RFC4655, august 2006.

[RFC4674] Le Roux, J.L., et al. "Requirements for PCE discovery", RFC4674, October 2006.

[RFC4205] Kompella, Rekhter, " IS-IS Extensions in Support of Generalized Multi-Protocol Label Switching (GMPLS)", RFC4205, October 2005.

[RFC3567] Li, T. and R. Atkinson, "Intermediate System to Intermediate System (IS-IS) Cryptographic Authentication", RFC 3567, July 2003.

12.2. Informative references

[RFC4657] Ash, J., Le Roux, J.L., " PCE Communication Protocol Generic Requirements", RFC4657, September 2006.

[PCEP] Vasseur et al., "Path Computation Element (PCE) communication Protocol (PCEP) - Version 1", draft-ietf-pce-pcep, work in progress.

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