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Carrying SR-Algorithm information in PCE-based Networks.

Abstract

The SR-Algorithm associated with a Prefix Segment-ID (SID) defines the path computation algorithm used by Interior Gateway Protocols (IGPs). This information is available to controllers such as the Path Computation Element (PCE) via topology learning. This document proposes an approach for informing headend routers regarding the SR-Algorithm associated with each Prefix SID used in PCE-computed paths, as well as signalling a specific SR-Algorithm as a constraint to the PCE.

Requirements Language

The key words "MUST", "MUST NOT", "REQUIRED", "SHALL", "SHALL NOT", "SHOULD", "SHOULD NOT", "RECOMMENDED", "NOT RECOMMENDED", "MAY", and "OPTIONAL" in this document are to be interpreted as described in BCP 14 [RFC2119] [RFC8174] when, and only when, they appear in all capitals, as shown here.

Status of This Memo

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Table of Contents

1. Introduction

A PCE can compute SR-TE paths using SIDs with different SR-Algorithms depending on the use-case, constraints, etc. While this information is available on the PCE, there is no method of conveying this information to the headend router.

Similarly, the headend can also compute SR-TE paths using different SR-Algorithms, and this information also needs to be conveyed to the PCE for collection or troubleshooting purposes. In addition, in the case of multiple (redundant) PCEs, when the headend receives a path from the primary PCE, it needs to be able to report the complete path information - including SR-Algorithm - to the backup PCE so that in HA scenarios, the backup PCE can verify the Prefix SIDs appropriately.

An operator may also want to constrain the path computed by the PCE to a specific SR-Algorithm, for example, in order to only use SR-Algorithms for a low-latency path. A new TLV is introduced for this purpose.

Valid SR-Algorithm values are defined in subregistry "IGP Algorithm Types" of "Interior Gateway Protocol (IGP) Parameters" IANA registry. Refer to Section 3.1.1 of [RFC8402] and [RFC9256] for definition of SR-Algorithm in Segment Routing. [RFC8665] and [RFC8667] are describing use of SR-Algorithm in IGP. Note that some RFCs are referring to SR-Algorithm with different names, for example "Prefix-SID Algorithm" and "SR Algorithm".

This document is extending:

* the SR PCE Capability Sub-TLV and the SR-ERO subobject - defined in [RFC8664]

* the SRv6 PCE Capability sub-TLV and the SRv6-ERO subobject - defined in [I-D.ietf-pce-segment-routing-ipv6]

A new TLV for signalling SR-Algorithm constraint to the PCE is also introduced, to be carried inside the LSPA object, which is defined in [RFC5440].

The mechanisms described in this document are equally applicable to both SR-MPLS and SRv6.

2. Terminology

The following terminologies are used in this document:

ASLA: Application-Specific Link Attribute.

BSID: Binding Segment Identifier.

ERO: Explicit Route Object.

FAD: Flexible Algorithm Definition.

IGP: Interior Gateway Protocol.

NAI: Node or Adjacency Identifier.

P2P: Point-to-Point.

P2MP: Point-to-Multipoint.

PCE: Path Computation Element.

PCEP: Path Computation Element Protocol.

SID: Segment Identifier.

SR: Segment Routing.

SR-TE: Segment Routing Traffic Engineering.

LSP: Label Switched Path.

LSPA: Label Switched Path Attributes.

Winning FAD: The FAD selected according to rules described in Section 5.3 of [RFC9350].

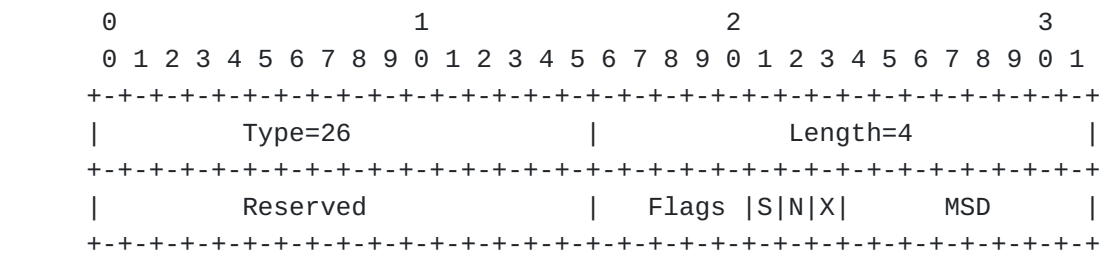
3. Object Formats

3.1. OPEN Object

3.1.1. SR PCE Capability Sub-TLV

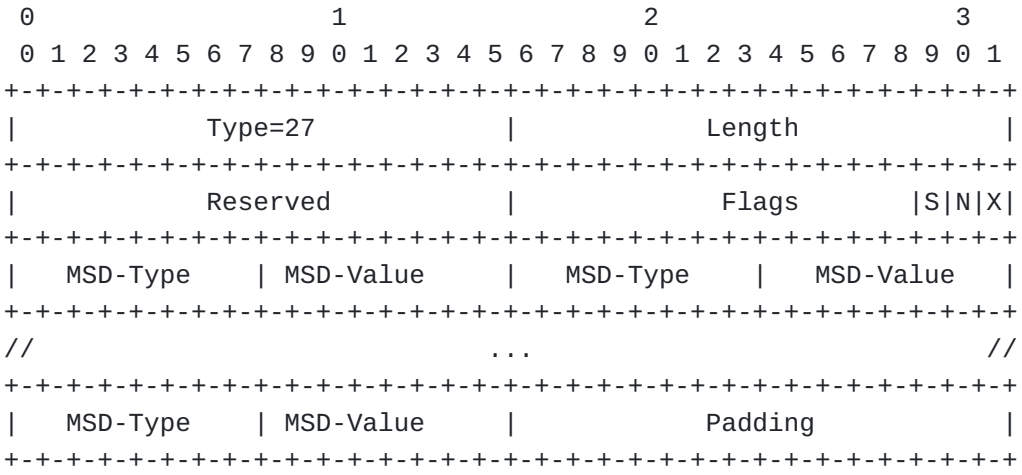
A new flag S is proposed in the SR PCE Capability Sub-TLV introduced in Section 4.1.2 of [RFC8664] to indicate support for SR-Algorithm. If S flag is set, PCEP peer indicates support for Algorithm field in SR-ERO Subject and SR-Algorithm constraint only for Traffic-

engineering paths with Segment Routing Path Setup Type. It is not indicating support for these extensions for other Path Setup Types.



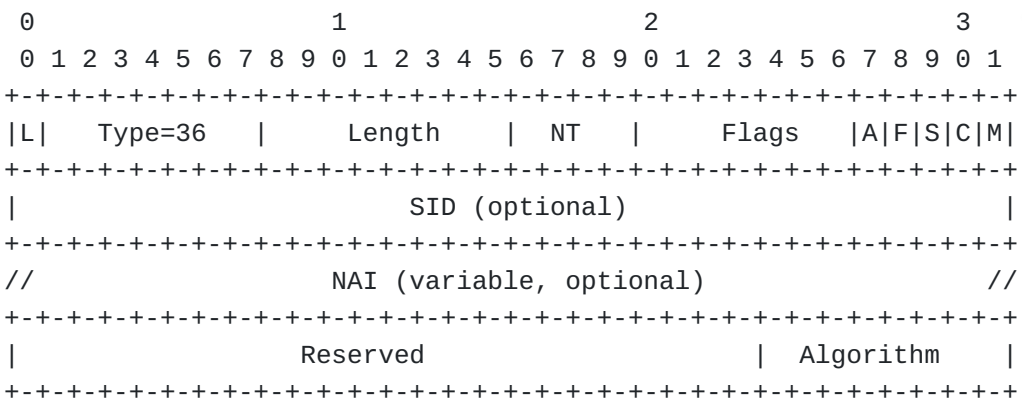
3.1.2. SRv6 PCE Capability sub-TLV

A new flag S is proposed in the SRv6 PCE Capability sub-TLV introduced in 4.1.1 of [I-D.ietf-pce-segment-routing-ipv6] to indicate support for SR-Algorithm. If S flag is set, PCEP peer indicates support for Algorithm field in SRv6-ERO Subobject and SR-Algorithm constraint only for Traffic-engineering paths with SRv6 Path Setup Type. It is not indicating support for these extensions for other Path Setup Types.



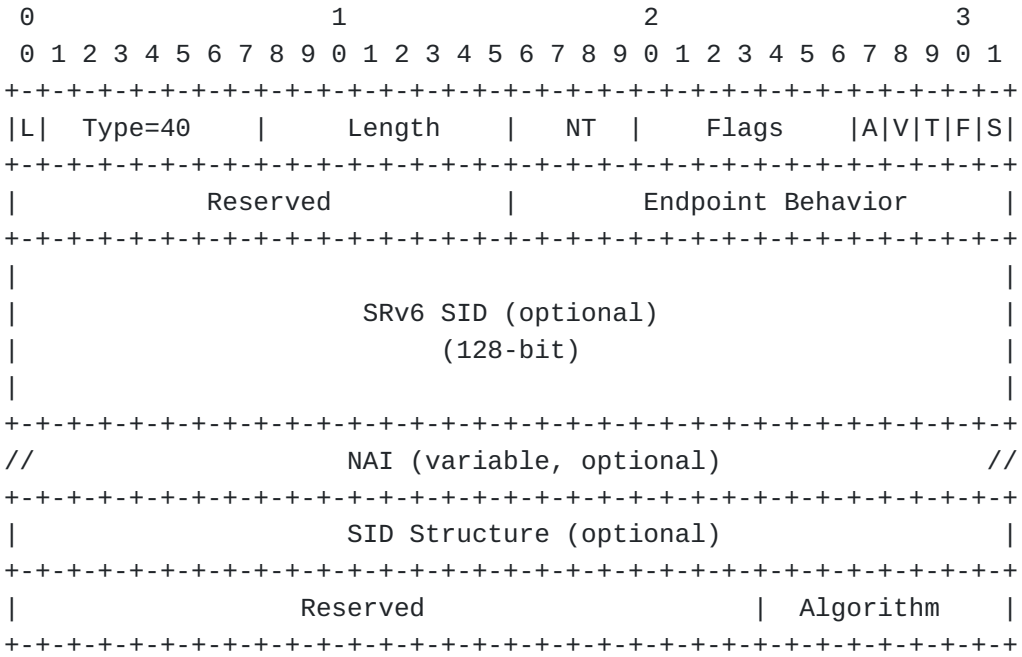
3.2. SR-ERO Subobject

The SR-ERO subobject encoding is extended with new flag "A" to indicate if the Algorithm field is included after other optional fields.



3.3. SRv6-ERO Subobject

The SRv6-ERO subobject encoding is extended with new flag "A" to indicate if the Algorithm field is included after other optional fields.



3.4. LSPA Object

A new TLV for the LSPA Object with TLV type=66 is introduced to carry the SR-Algorithm constraint. This TLV SHOULD only be used when PST (Path Setup type) = SR or SRv6. Only the first instance of this TLV SHOULD be processed, subsequent instances SHOULD be ignored

The format of the SR-Algorithm TLV is as follows:

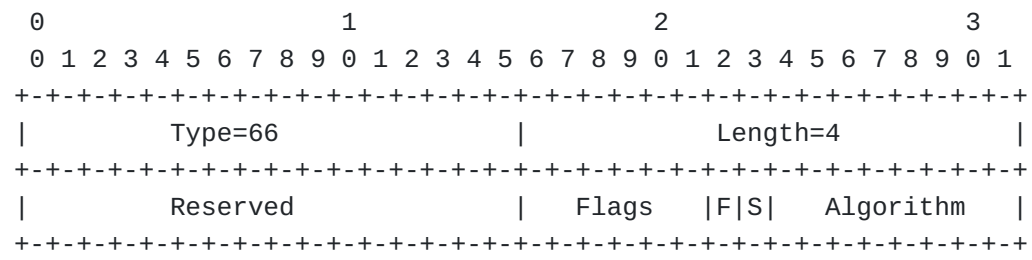


Figure 1: SR-Algorithm TLV Format

The code point for the TLV type is 66. The TLV length is 4 octets.

The 32-bit value is formatted as follows.

Reserved: MUST be set to zero by the sender and MUST be ignored by the receiver.

Flags: This document defines the following flag bits. The other bits MUST be set to zero by the sender and MUST be ignored by the receiver.

*S (Strict): If set, the PCE MUST fail the path computation if specified SR-Algorithm constraint cannot be satisfied. If unset, the PCE MAY ignore specified algorithm constraint.

*F (Flexible Algorithm Path Computation): If set, the PCE follows procedures defined in Section 4.2.1. If unset, the PCE follows procedures defined in Section 4.2.2. The flag SHOULD be ignored if Algorithm field is set to value in range 0 to 127.

Algorithm: SR-Algorithm the PCE MUST take into acount while computing a path for the LSP.

3.5. Extensions to METRIC Object

The METRIC object is defined in Section 7.8 of [RFC5440] This document defines the following types for the METRIC object.

*T:22: Path Min Delay metric (Section 3.5.1)

*T:23: P2MP Path Min Delay metric (Section 3.5.2)

3.5.1. Path Min Delay Metric

[RFC7471] and [RFC8570] defined as "Min Unidirectional Link Delay". The Min Link Delay metric represents measured minimum link delay value over a configurable interval.

The Path Min Delay metric type of the METRIC object in PCEP represents the sum of the Min Link Delay metric of all links along a P2P path.

*A Min Link Delay metric of link L is denoted D(L).

*A path P of a P2P LSP is a list of K links {Lpi,(i=1...K)}.

*A Path Min Delay metric for the P2P path P = Sum {D(Lpi), (i=1...K)}.

3.5.2. P2MP Path Min Delay Metric

The P2MP Path Min Delay metric type of the METRIC object in PCEP encodes the Path Min Delay metric for the destination that observes the worst delay metric among all destinations of the P2MP tree.

*A P2MP tree T comprises a set of M destinations {Dest_j, (j=1...M)}.

*The P2P Path Min Delay metric of the path to destination Dest_j is denoted by PMDM(Dest_j).

*The P2MP Path Min Delay metric for the P2MP tree T = Maximum{PMDM(Dest_j), (j=1...M)}.

3.5.3. Path Min Delay Metric value

[RFC7471] and [RFC8570] define "Min/Max Unidirectional Link Delay Sub-TLV" to advertise the link minimum and maximum delay in microseconds in a 24-bit field.

[RFC5440] defines the METRIC object with a 32-bit metric value encoded in IEEE floating point format.

The encoding for the Path Min Delay metric value is quantified in units of microseconds and encoded in IEEE floating point format.

The conversion from 24-bit integer to 32-bit IEEE floating point could introduce some loss of precision.

4. Operation

The PCEP protocol extensions defined in Sections 3.2, 3.3 and 3.4 of this draft MUST NOT be used if one or both PCEP speakers have not indicated the support using S flag in Path Setup Type specific Sub-TLVs in their respective OPEN messages.

SR-Algorithm used in this document refers to complete range of SR-Algorithm values (0-255) if specific section does not specify otherwise.

4.1. SR-ERO and SRv6-ERO Encoding

PCEP speaker MAY set the A flag and include the Algorithm field in SR-ERO or SRv6-ERO subobject if the S flag was advertised by both PCEP speakers.

If PCEP peer receives SR-ERO subobject with the A flag set or with the SR-Algorithm included, but the S flag was not advertised, then it MUST consider entire ERO as invalid as described in Section 5.2.1 of [RFC8664]

The Algorithm field MUST be included after optional SID, NAI or SID structure and length of SR-ERO or SRv6-ERO subobject MUST be increased with additional 4 bytes for Reserved and Algorithm field.

If the length and the A flag are not consistent, it MUST consider the entire ERO invalid and MUST send a PCErr message with Error-Type = 10 ("Reception of an invalid object") and Error-value = 11 ("Malformed object").

4.2. SR-Algorithm Constraint

In order to signal a specific SR-Algorithm constraint to the PCE, the headend MUST encode the SR-Algorithm TLV inside the LSPA object.

If PCEP peer receives LSPA object with SR-Algorithm TLV in it, but the S flag was not advertised, then PCEP peer MUST ignore it as per Section 7.1 of [RFC5440].

Path computation MUST occur on the topology associated with specified SR-Algorithm. The PCE MUST NOT use Prefix SIDs of SR-Algorithm other than specified in SR-Algorithm constraint. It is allowed to use other SID types (e.g., Adjacency or Binding SID), but only from nodes participating in specified SR-Algorithm.

Specified SR-Algorithm constraint is applied to end-to-end SR policy path. Using different SR-Algorithm constraint in each domain or part of the topology in single path computation is out of scope of this document. One possible solution is to determine FAD mapping using PCE local policy.

If the PCE is unable to find a path with the given SR-Algorithm constraint or it does not support combination of specified constraints, it MAY respond with PCInitiate or PCUpdate message with empty ERO or PCRep with NO-PATH object to indicate that it was not able to find valid path.

If headend is part of multiple IGP domains and winning FAD for specified SR-Algorithm in each of them has different constraints, the PCE implementation MAY have local policy with defined behavior for selecting FAD for such path-computation or even completely not supporting it. It is RECOMMENDED to respond with PCInitiate or PCUpdate message with empty ERO or PCRep with NO-PATH object if such path-computation is not supported.

If NO-PATH object is included in PCRep, then PCE MAY include SR-Algorithm TLV to indicate constraint, which cannot be satisfied as described in section 7.5 of [RFC5440].

SR-Algorithm does not replace the Objective Function defined in [RFC5541]

4.2.1. Flexible Algorithm Path computation

This section is applicable only to Flexible Algorithms range of SR-Algorithm values.

The PCE MUST follow IGP Flexible Algorithm path computation logic as described in [RFC9350]. That includes using same ordered rules to select FAD if multiple FADs are available, considering node participation of specified SR-Algorithm in the path computation, using ASLA specific link attributes and other rules for Flexible Algorithm path computation described in that document.

The PCE MUST optimize computed path based on metric type specified in the FAD, metric type included in PCEP messages from PCC MUST be ignored. The PCE SHOULD use metric type from FAD in messages sent to the PCC. If corresponding metric type is not defined in PCEP, PCE SHOULD skip encoding of metric object for optimization metric.

There are corresponding metric types in PCEP for IGP and TE metric from FAD introduced in [RFC9350], but there was no corresponding metric type defined for "Min Unidirectional Link Delay". Section 3.5 of this document is introducing it.

The PCE MUST use constraints specified in the FAD and also constraints directly included in PCEP messages from PCC. The PCE implementation MAY decide to ignore specific constraints received from PCC based on existing processing rules for PCEP Objects and TLVs, e.g. P flag described in Section 7.2 of [RFC5440] and processing rules described in [I-D.ietf-pce-stateful-pce-optional]. If the PCE does not support specified combination of constraints, it MAY respond with PCEP message with PCInitiate or PCUpdate message with empty ERO or PCRep with NO-PATH object. PCC MUST NOT include constraints from FAD in PCEP message sent to PCE as it can result in undesired behavior in various cases. PCE SHOULD NOT include constraints from FAD in PCEP messages sent to PCC.

4.2.2. Path computation with SID filtering

The SR-Algorithm constraint acts as a filter, restricting which SIDs may be used as a result of the path computation function. Path computation is done based on optimization metric type and constraints specified in PCEP message received from PCC.

If specified SR-Algorithm is Flexible Algorithm, the PCE MUST ensure that IGP path of Flexible Algorithm SIDs is congruant with computed path.

4.2.3. New Metric types

All the rules of processing the METRIC object as explained in [RFC5440] and [RFC8233] are applicable to new metric types defined in this document.

5. Manageability Considerations

All manageability requirements and considerations listed in [RFC5440], [RFC8231] and [RFC8281] apply to PCEP protocol extensions defined in this document. In addition, requirements and considerations listed in this section apply.

5.1. Control of Function and Policy

A PCE or PCC implementation MAY allow the capability of supporting PCEP extensions introduced in this document to be enabled/disabled as part of the global configuration.

5.2. Information and Data Models

An implementation SHOULD allow the operator to view the capability defined in this document. Section 4.1 and 4.1.1 of [I-D.ietf-pce-pcep-yang] should be extended to include that capabilities introduced in Section 3.1.1 and 3.1.2 for PCEP peer.

5.3. Verify Correct Operations

Operation verification requirements already listed in [RFC5440], [RFC8231], [RFC8281] and [RFC8664] are applicable to mechanisms defined in this document.

An implementation SHOULD also allow the operator to view FADs, which MAY be used in Flexible Algorithm path computation defined in Section 4.2.1.

An implementation SHOULD allow the operator to view nodes participating in specified SR-Algorithm.

5.4. Impact On Network Operations

The mechanisms defined in [RFC5440], [RFC8231], and [RFC8281] also apply to the PCEP extensions defined in this document.

6. Implementation Status

[Note to the RFC Editor - remove this section before publication, as well as remove the reference to RFC 7942.]

This section records the status of known implementations of the protocol defined by this specification at the time of posting of this Internet-Draft, and is based on a proposal described in [RFC7942]. The description of implementations in this section is intended to assist the IETF in its decision processes in progressing drafts to RFCs. Please note that the listing of any individual implementation here does not imply endorsement by the IETF. Furthermore, no effort has been spent to verify the information presented here that was supplied by IETF contributors. This is not intended as, and must not be construed to be, a catalog of available implementations or their features. Readers are advised to note that other implementations may exist.

According to [RFC7942], "this will allow reviewers and working groups to assign due consideration to documents that have the benefit of running code, which may serve as evidence of valuable experimentation and feedback that have made the implemented protocols more mature. It is up to the individual working groups to use this information as they see fit".

6.1. Cisco

*Organization: Cisco Systems

*Implementation: IOS-XR PCC and PCE.

*Description: SR-MPLS part with experimental codepoints.

*Maturity Level: Production.

*Coverage: Partial.

*Contact: ssidor@cisco.com

7. Security Considerations

The security considerations described in [RFC5440], [RFC8231], [RFC8253],[RFC8281],[RFC8664] and [RFC9350] in itself.

Note that this specification introduces possibility to compute paths by PCE based on Flexible Algorithm related topology attributes and based on metric type and constraints from FAD. This creates additional vulnerabilities, which are already described for path computation done by IGP like those described in Security Considerations section of [RFC9350], but which are also applicable to path computation done by PCE.

8. IANA Considerations

8.1. SR Capability Flag

IANA maintains a sub-registry, named "SR Capability Flag Field", within the "Path Computation Element Protocol (PCEP) Numbers" registry to manage the Flags field of the SR-PCE-CAPABILITY TLV. IANA is requested to make the following assignment:

Bit	Description	Reference
5	SR-Algorithm Capability	This document

Table 1

8.2. SRv6 PCE Capability Flag

IANA was requested in [I-D.ietf-pce-segment-routing-ipv6] to create a sub-registry, named "SRv6 PCE Capability Flags", within the "Path Computation Element Protocol (PCEP) Numbers" registry to manage the Flags field of SRv6-PCE-CAPABILITY sub-TLV. IANA is requested to make the following assignment:

Bit	Description	Reference
TBD1	SR-Algorithm Capability	This document

Table 2

8.3. SR-ERO Flag

IANA maintains a sub-registry, named "SR-ERO Flag Field", within the "Path Computation Element Protocol (PCEP) Numbers" registry to manage the Flags field of the SR-ERO Subobject. IANA is requested to make the following assignment:

Bit	Description	Reference
7	SR-Algorithm Flag	This document

Table 3

8.4. SRv6-ERO Flag

IANA was requested in [I-D.ietf-pce-segment-routing-ipv6], named "SRv6-ERO Flag Field", within the "Path Computation Element Protocol (PCEP) Numbers" registry to manage the Flags field of the SRv6-ERO subobject. IANA is requested to make the following assignment:

Bit	Description	Reference
TBD2	SR-Algorithm Flag	This document

Table 4

8.5. PCEP TLV Types

IANA maintains a subregistry, named "PCEP TLV Type Indicators", within the "Path Computation Element Protocol (PCEP) Numbers" registry. IANA is requested to allocate a new TLV type for the new LSPA TLV specified in this document.

Type	Description	Reference
66	SR-Algorithm	This document

Table 5

8.6. Metric Types

IANA maintains a subregistry for "METRIC Object T Field" within the "Path Computation Element Protocol (PCEP) Numbers" registry. IANA is requested to allocate a new values for metric types defined in this document:

Type	Description	Reference
22	Path Min Delay Metric	This document
23	P2MP Path Min Delay Metric	This document

Table 6

9. References

9.1. Normative References

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9.2. Informative References

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