IETF 105 – Montreal
Jul 2019

SR Generic FEC TLV for LSP Ping

(draft-nainar-mpls-spring-lsp-ping-sr-generic-sid)

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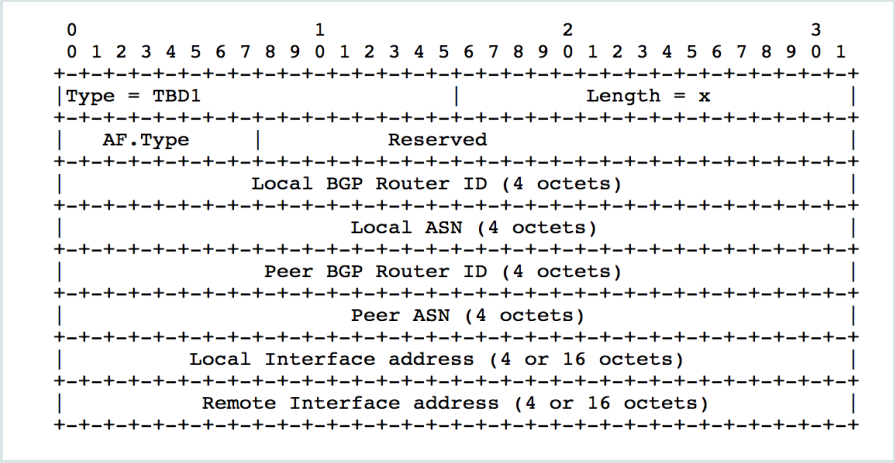
Problem Statement

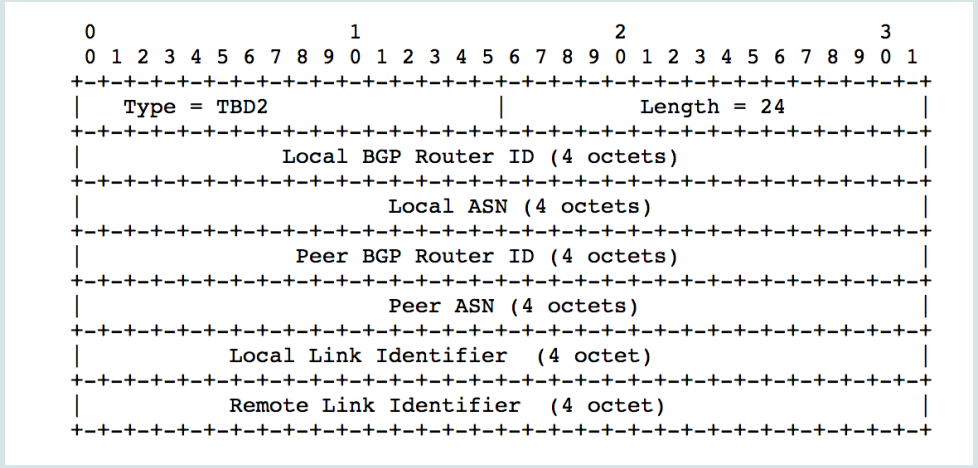
- Requires new target FEC Stack sub-TLV definition and standardization efforts for each new Segment ID defined.
  - Define new TLV.
  - Update FEC validation procedure of RFC-8029
- Requires domain/node wide software upgrade depending on the type of the Segment ID defined.
- Raises usability and scalability challenges.

Problem Statement (A partial list of New SR FECs)

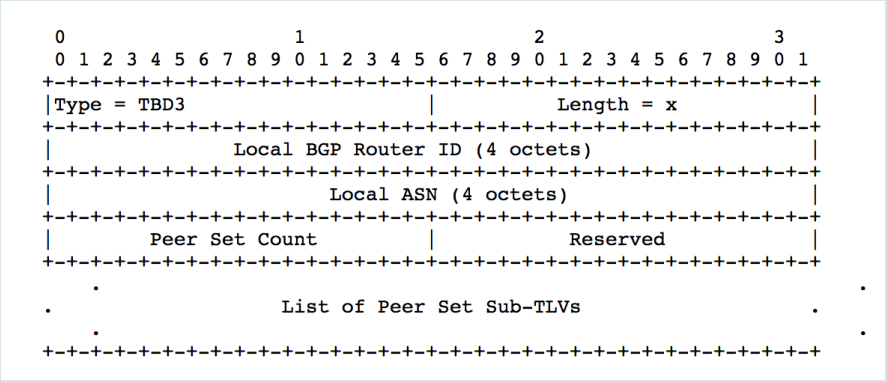
BGP Peer Node SID



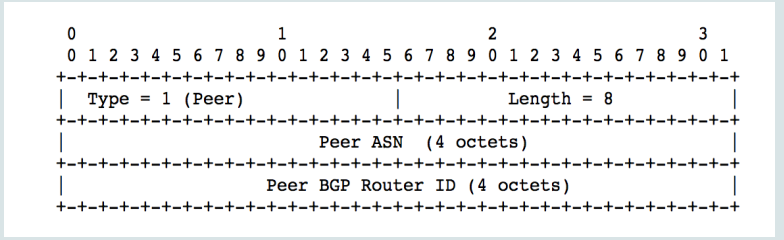
BGP Peer Adj-SID

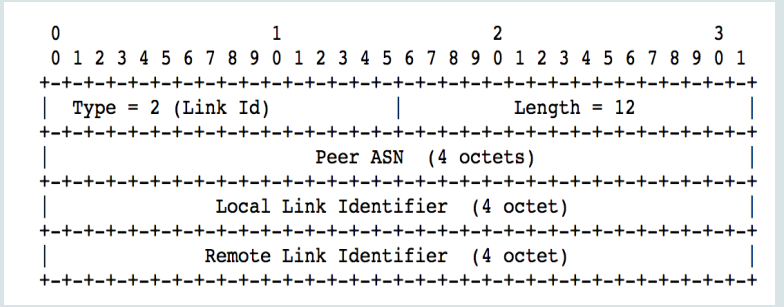


BGP Peer Set SID

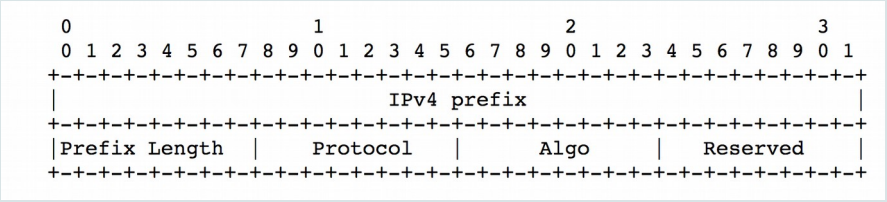


BGP Peer Set SID Sub-TLVs



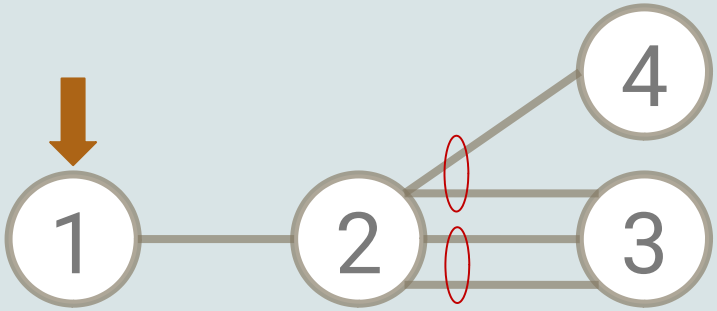


FEC changes for Flex-Algo



Problem Statement (Cont'ed)

- Complex validation procedures at Egress (one for each SID type).
- Requires a lot of information to be derived by the Initiator to include in the Echo Request.
- Complex FEC filling procedures at Ingress (one for each SID type).
- In some cases, ingress is unable to fill-in the required information.
  - E.g., Initiator of ping (node 1) does not know how the packet will be load balanced at a target node (node 2).



Solution

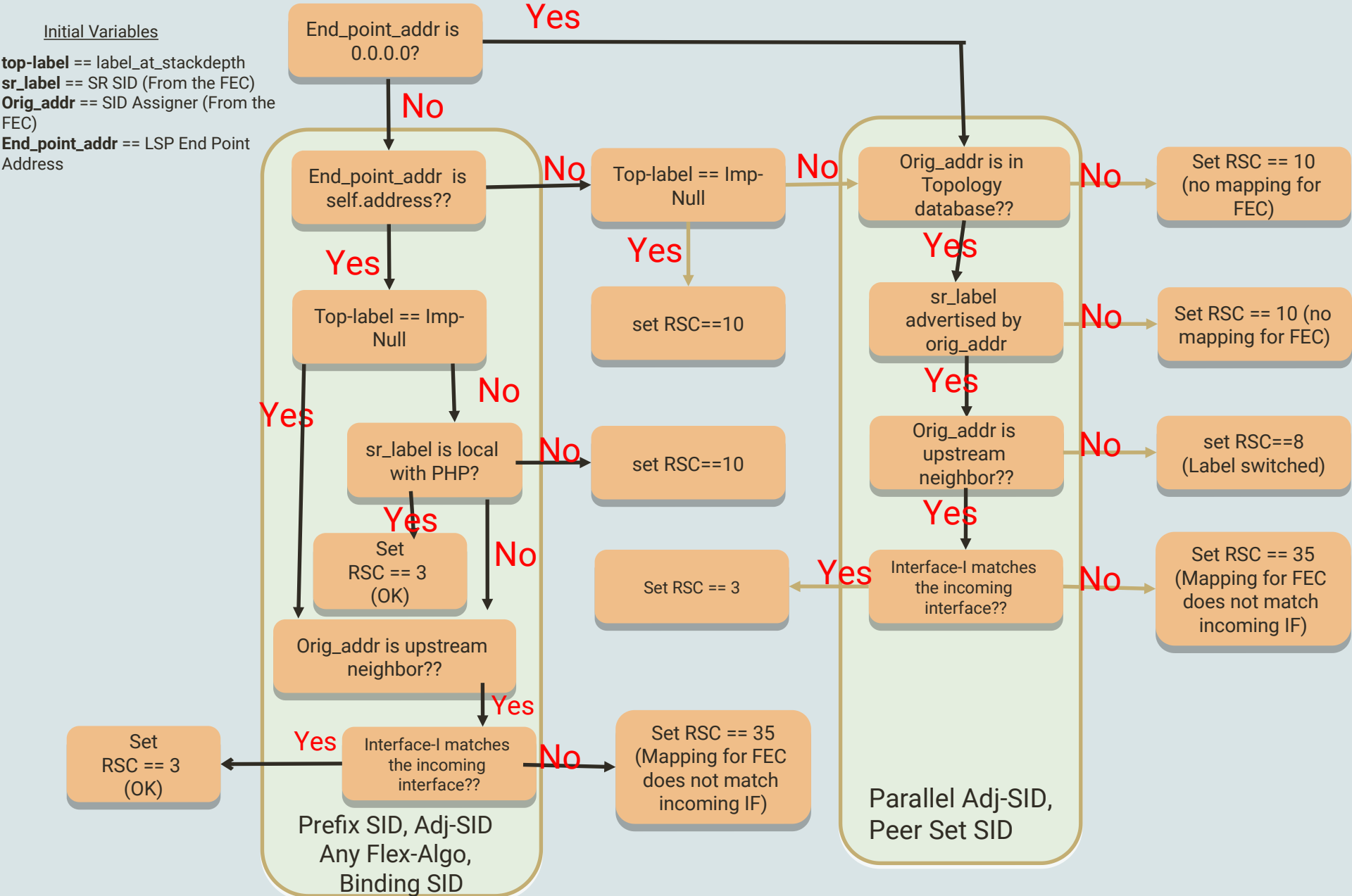
- SR SID data model is:
  - Segment ID (Label)
  - SID Assigner
- Define a SID based on the SR SID data model and use it for all various SID types.

SR Generic Label Sub-TLV

SR SID (20 Bits)
SID Assigner
LSP End Point (Optional; may be 0.0.0.0)

- SR SID
  - Carries 20 bits of Segment ID used for validation.
- SID Assigner
  - Node address of the Segment ID assigner.
- LSP End Point
  - Node address of the endpoint that terminates the LSP.
  - LSP End Point may be set to 0.0.0.0 by the initiator.
    - E.g., for parallel adjacency.
  - If LSP End Point address is set, the Egress MAY skip the SID assigner check.
    - E.g., for BSID

Responder behavior (New)



Procedure

Prefix SID Validation

16000x ␣ Prefix SID for Rx for Algo 0
16128x ␣ Prefix SID for Rx for Algo 128

- Initiator (R1) triggers LSP Ping with below SR Generic Label Sub-TLV:
  - For Prefix SID 160008 {SID=160008; SID Assigner = R8; LSP-EndPoint = R8}
  - For Prefix SID 161288 {SID=161288; LSP-EndPoint = R8}
- R8 validates if LSP-EndPoint == self; and if 160008 is assigned locally.

Procedure

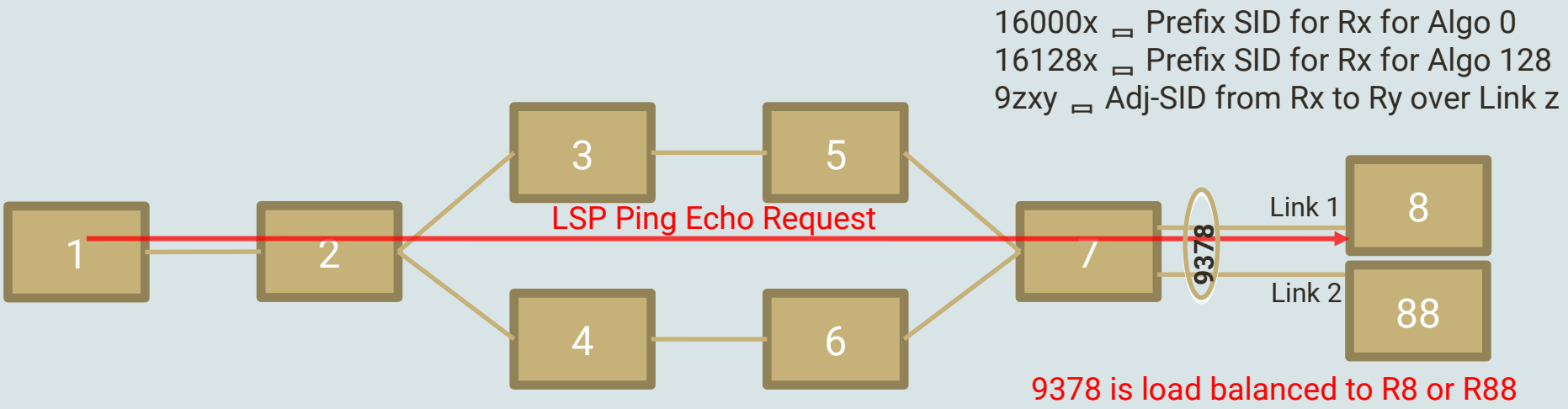
Parallel Adj-SID Validation

16000x ␣ Prefix SID for Rx for Algo 0
16128x ␣ Prefix SID for Rx for Algo 128
9zxy ␣ Adj-SID from Rx to Ry over Link z

- Initiator (R1) triggers LSP Ping with below SR Generic Label Sub-TLV:
  - For Parallel Adj SID 9378 {SID=9378; SID Assigner = R7; LSP-EndPoint = R8}
- R8 validates if LSP-EndPoint == self; and if Inteface-I matches interface for 9378.

Procedure

Parallel Adj-SID Validation



- Initiator (R1) triggers LSP Ping with below SR Generic Label Sub-TLV:
  - For Parallel Adj SID 9378 {SID=9378; SID Assigner = R7; LSP-EndPoint = 0.0.0.0}
- Responder (R8 or R88) validates if SID Assigned==upstream; validates if Inteface-I matches interface for 9378.

In a nut shell

- One Target FEC Stack Sub-TLV that covers multiple Segment IDs.
- Drastically reduces the information required on the Initiator.
  - Ease of operation.
- Reduces the information to be processed by the responder.
- Extendable to accommodate future Segment IDs.

IANA Registry Allocation

- Request for a new Sub-TLV for TLV types 1, 16 and 21.
- Value from range 38-31743 (Unassigned range)
- Re-uses existing Return codes and Return Sub-codes

MPLS or SPRING WG?

- It is really up to the chairs to decide.

I-D Status

- Next Steps:
  - WG feedback sought
  - Textual Contributions Welcomed!
  - WG Adoption after Montreal
- Thank you!