SR Generic FEC TLV for LSP Ping

(draft-nainar-mpls-spring-lsp-ping-sr-generic-sid)

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Problem Statement

- Requires new target FEC Stack sub-TLV definition and standardization efforts for each new Segment ID defined.
  - Define new TLV.
  - Update FEC validation procedure of RFC-8029

- Requires domain/node wide software upgrade depending on the type of the Segment ID defined.

- Raises scalability challenges.
Problem Statement (A partial list of New SR FECs)

- BGP Peer Node SID
- BGP Peer Adj-SID
- BGP Peer Set SID
- BGP Peer Set SID Sub-TLVs
- FEC changes for Flex-Algo
Problem Statement (Cont’ed)

- Requires a lot of information to be derived by the Initiator to include in the Echo Request.
- Complex FEC filling procedures at Ingress (one for each Prefix SID type).
- Complex validation procedures at Egress (one for each Prefix SID type).
Solution

- **SR SID data model is:**
  - Segment ID (Label)
  - SID Assigner

- **FEC validation Procedure**
  - Segment ID to Interface mapping is maintained by any node.
    - Local implementation matter
  - Initiator defines the SID value and LSP EndPoint while triggering LSP Ping
    - Manually defined via CLI or dynamic PCE query.
  - Responder validates the LSP End Point and incoming interface.
    - Respond based on the validation.
## SR Generic Label Sub-TLV

<table>
<thead>
<tr>
<th>SR SID (20 Bits)</th>
<th>LSP End Point (Optional; may be 0.0.0.0)</th>
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- **SR SID**
  - Carries 20 bits of Segment ID used for validation.

- **LSP End Point**
  - Node address of the endpoint that terminates the LSP.
  - LSP End Point may be set to 0.0.0.0 by the initiator.
    - E.g., for parallel adjacency.
  - If LSP End Point address is set, the Egress MAY skip the SID assigner check.
    - E.g., for BSID
Responder behavior

Pre-fix SID
Any flex-algo

Top-label == label_at_stackdepth
sr_label == SR-Label
orig_addr == Assigner
Interface-I == incoming_intf

Orig_addr is self.address??

Yes
No

sr_label is in local database??

Yes
No

Top-label == Imp-Null

Yes
No

set RSC==10

sr_label advertised by orig_addr

Yes
No

set RSC==8 (Label switched)

sr_label == adj-sid??

Yes
No

Orig_addr is upstream neighbor??

Yes
No

Set RSC == x1 (mal func echo)

Interface-I matches the incoming interface??

Yes
No

Set RSC == 35 (Mapping for FEC does not match incoming IF)

Set RSC == 10 (no mapping for FEC)

Set RSC == 3 (OK)

Set RSC == 8 (Label switched)

Set RSC == 10 (no mapping for FEC)
R8 maintains the below mapping:

- **160008** → Incoming Interface: {Any}
- **161288** → Incoming Interface: {{Any}
- **9178** → Incoming Interface: {Link 1}
- **9278** → Incoming Interface: {Link 2}
- **9378** → Incoming Interface: {Link 1 or Link 2}
Procedure
Initiator Behavior

- Initiator (R1) triggers LSP Ping with below SR Generic Label Sub-TLV:
  - For Prefix SID 160008 {SID=160008; LSP-EndPoint = R8}
  - For Prefix SID 161288 {SID=161288; LSP-EndPoint = R8}
  - For ADJ-SID 9178 {SID=9178; LSP-EndPoint = R8}
  - For ADJ-SID 9278 {SID=9278; LSP-EndPoint = R8}
  - For ADJ-SID 9378 {SID=9378; LSP-EndPoint = R8}
Responder (R8) uses SID, LSP Endpoint info and the local mapping for validation.

- LSP EndPoint == self?
- Incoming_Interface matches the local table?

Sends positive/negative response accordingly.
In a nut shell

- One Target FEC Stack Sub-TLV that covers multiple Segment IDs.
  - Prefix/Flex-Algo/Adj/ePE SIDs

- Drastically reduces the information required on the Initiator.
  - Ease of operation.

- Reduces the information to be processed by the responder.

- Extendable to accommodate future Segment IDs.
IANA Registry Allocation

- Request for a new Sub-TLV for TLV types 1, 16 and 21.
- Value from range 38-31743 (Unassigned range)
- Re-uses existing Return codes and Return Sub-codes
I-D Status

Next Steps:
- WG feedback sought
- Textual Contributions Welcomed!
- WG Adoption in MPLS WG

Thank you!