

DC aware TE topology model

draft-llc-teas-dc-aware-topo-model-00

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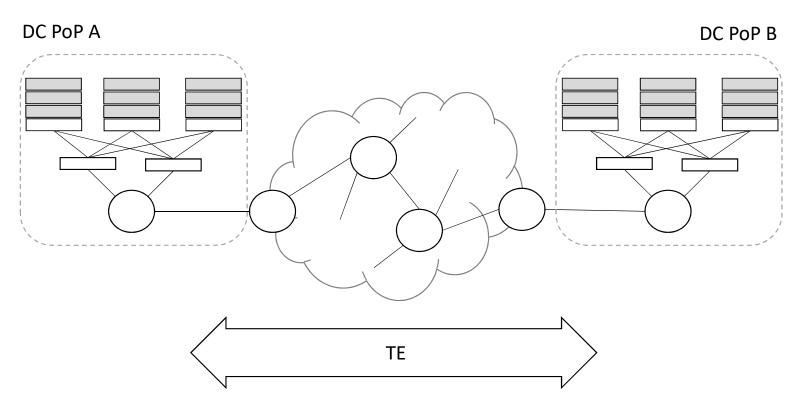
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Problem statement

- Wide deployment of computing facilities across service provider's Networks, in the form of DC PoPs
- Interesting to have joint topological view of both networking and computing resources available
 - It can assist on TE decisions that could require combined awareness of network and compute domains
- Similar approach as the one followed in *draft-ietf-teas-sf-aware-topo-model* but concentrated on available resources instead of functions

Scenario



- DC PoPs described in terms of resource capabilities such as CPU, memory, storage, etc
- Alternatively, they could be described in terms of resource bundles (quotas, flavors), e.g. CNTT

IETF#109, Online meeting, November 2020

CNTT -- Common Network Function
Virtualisation Infrastructure Telecom Taskforce
(https://cntt-n.github.io/CNTT/doc/ref_model/)

Proposal

 To provide a model for characterizing the compute domain information per DC PoP, integrated with the topological information of the network

```
module: ietf-dcpop-dc
    +--rw dcpop
       +--rw dc* [id]
          +--rw hypervisor* [id]
             +--rw ram
                              uint32
                +--rw total?
               +--rw used?
                              uint32
               +--rw free?
                              uint32
             +--rw disk
               +--rw total? uint32
                              uint32
               +--rw used?
              +--rw free?
                              uint32
             +--rw vcpu
               +--rw total? uint16
                              uint16
               +--rw used?
               +--rw free?
                              uint16
             +--rw instance*
                              -> /dcpop/dc/instance/id
             +--rw id
                              string
             +--rw name?
                              string
          +--rw instance* [id]
             +--rw flavor
                +--rw disk?
                              uint32
             +--rw ram?
                              uint32
              +--rw vcpus?
                              uint16
               +--rw id?
                              string
```

Next steps

- Adapt the model to different ways of exposing DC capabilities
- Work on the YANG modules accompanying such model
- Any feedback / comment is more than welcome