



MSPL FOR FA

draft-kompella-mpls-mspl4fa
ietf 113 (vienna)

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functionally, pretty stable

- Need WG to make some decisions
 - These have been on the table for a while now, so shouldn't take long
- After that (or in parallel), adopt the doc as a WG document
- Then, get down to nailing down
 - Backward compatibility
 - Extensibility
 - Bit formats
 - IANA (allocation) details
 - Deployment strategies

three key contributions

1. Use a single SPL for multiple purposes (running out of labels)
2. Use the full label entry (i.e., include TC/TTL fields) for efficiency
3. Encode forwarding actions succinctly for efficiency

1. use “in-stack data”?

- This should be obvious, but there’s a constant undertone that all “MIAD” data MUST be in PSD
- Number of reasons to use ISD:
 1. Reaching BoS can be expensive or impossible, esp. for legacy equipment
 2. Even if possible, more efficient to use ISD for data critical for correct forwarding

Can the WG give feedback on the use of ISD?
Can we arrive at WG consensus on guidelines
on when to use ISD vs. PSD?

our suggestion


Yes, do!
(use guidelines
in draft)

2. repeat ISD in PSD?

Can the WG give feedback on whether there is value in repeating the ISD in the PSD?

Not worth it

3. approach is efficient & extensible

- an action is encoded in a single bit (usually)
 - **0**: don't do the action + no associated data; **1**: do it + there may be associated data
 - the number of flag bits is extensible
 - the associated data for a flag is stated as part of the IANA registry
 - typically, 0 or 4 octets
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Can the WG ratify that the approach is efficient and extensible, and the ISD data limit works?

4. a 2-bit flag for EG?

- the exception to the 1 bit = 1 action and 0-4 bytes of data is EG
- EG is a 2-bit flag combining the Entropy Label and the Slice ID, allowing for more combinations of sizes for each
- “clever” – too clever?

Does the WG have opinions on whether the flexibility of EL/GIS sizes is worth the complexity?

5. can mspl4fa reach ToS?

- it may be more convenient and more efficient to allow the “FAI” SPL to reach the top-of-stack. there are three approaches:
 1. Never let this happen: an LSR that pops a label and sees that the next label is the “FAI” label MUST pop the FAI and all associated data
 2. Allow this to happen: next LSR MUST be able to deal with the FAI label
 3. Push a neutral label on top of the FAI (e.g., label 0)

This doesn't have to be decided right away.
WG thoughts on directions?

next steps

- Bit-wrangling: “continuation bits” vs. explicit length
- Bit positions for forwarding actions
- Detailed IANA section
- Procedures
 - dealing with legacy equipment
 - computing “safe” paths
 - error handling
 - "what could go wrong?"
- Get WG feedback on questions (slides 4-7)
- WG adoption