



DC aware TE topology model

draft-llc-teas-dc-aware-topo-model-02

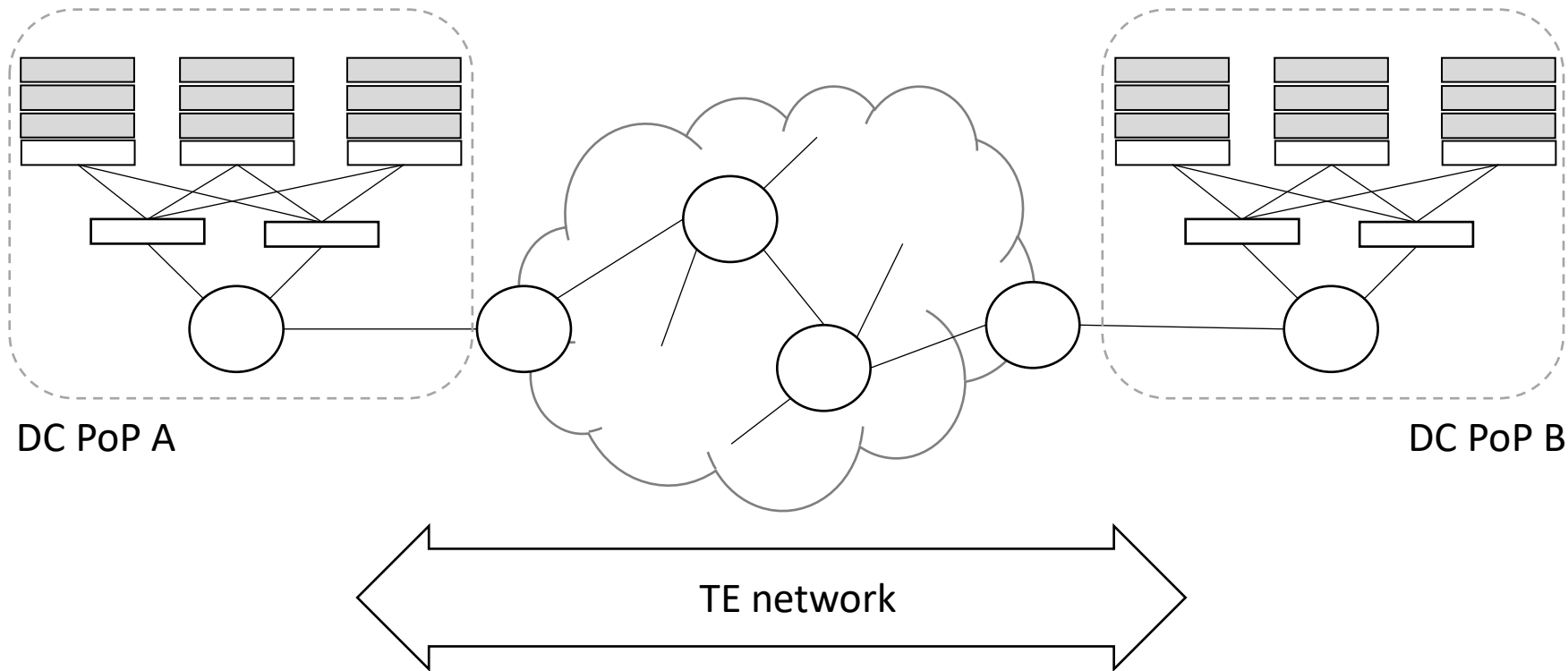
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Problem statement

- Wide deployment of computing facilities across service provider's Networks, in the form of DC PoPs
- Interesting to have joint topological view of both networking and computing resources available to assist on TE decisions that could require combined awareness of network and compute domains
- Similar approach as the one followed in *draft-ietf-teas-sf-aware-topo-model* but concentrated on available DC resources instead of functions



- DC PoPs described in terms of resource capabilities such as CPU, memory, storage, etc
- Alternatively, they could be described in terms of resource bundles (quotas, flavors), e.g. CNTT

CNTT "Cloud iNfrastructure Telco Taskforce Reference Model, Reference Architectures",
https://cntt.readthedocs.io/en/stable-elbrus/ref_arch/README.html/

Proposal

- To provide a model for characterizing the compute domain information per DC PoP, integrated with the topological information of the network

Flavor	vCPU	RAM	Storage	Bandwidth
.tiny	1	512 MB	1 GB	1 Gbps
.small	1	2 GB	20 GB	1 Gbps
.medium	2	4 GB	40 GB	1 Gbps
.large	4	8 GB	80 GB	1 Gbps
.2xlarge	8	16 GB	160 GB	1 Gbps
.4xlarge	16	32 GB	320 GB	1 Gbps
.8xlarge	32	64 GB	640 GB	1 Gbps

Table 1: Predefined Compute Flavors

Besides the predefined flavors, it is also possible to use customized (i.e. parameterized) flavors.

```
module: ietf-dcpop-dc
  +--rw dcpop
    +--rw dc* [id]
      | +--rw hypervisor* [id]
      | | +--rw ram
      | | | +--rw total? uint32
      | | | +--rw used? uint32
      | | | +--rw free? uint32
      | | +--rw disk
      | | | +--rw total? uint32
      | | | +--rw used? uint32
      | | | +--rw free? uint32
      | | +--rw vcpu
      | | | +--rw total? uint16
      | | | +--rw used? uint16
      | | | +--rw free? uint16
      | | +--rw instance* -> /dcpop/dc/instance/id
      | | +--rw id string
      | | +--rw name? string
      | +--rw instance* [id]
      | | +--rw flavor
      | | | +--rw disk? uint32
      | | | +--rw ram? uint32
      | | | +--rw vcpus? uint16
      | | | +--rw id? string
      :
      :
      :
```

Summary

- Version -00 presented at IETF 109
- Versions -01 and -02 provide updates mainly on the structure of the compute flavors
- As next steps:
 - Adapt the model to different ways of exposing DC capabilities
 - Work on the YANG modules accompanying such model
- Any feedback / comment is more than welcome