

# Cyclic Queuing and Forwarding for DetNet IP and MPLS Data Plane (TCQF)

...and BIER-TE...

## draft-eckert-detnet-tcwf-02

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# Changes from -01 (IETF115)

- Review David Black (after DetNetWG meeting)
- Concern about pseudocode/explanation to be implying stricter than necessary forwarding rules
  - Pseudocode showed strict arrival time based serialization on output FIFO – First in on input, First out on output cycle buffer
- What do we want ?
  - TCQF itself would work perfectly work well with packets within single cycle buffer be arbitrarily reordered.
  - BUT: Any end-to-end flow with more than one packet within a cycle could experience packet reordering if we did this
- Revision -02:
  - Conservative approach: specify that we maintain order fom

# Changes from -01 (IETF115)

Conservative approach: specify that we maintain order between packets arriving from the same input interface and going to the same output interface / cycle

```
while(1) {
    ingress_flow_2_tcqf(oif,cycle) // [5]
    wait_until(tnow >= nextcyclestart); // wait until next cycle
    nextcyclestart += tcqf.cycle_time
    forall(iif) {
        forall(pak = tcqf_dequeue(oif.cycleq[cycle,iif]) {
            schedule to send pak on oif before nextcyclestart; // [4]
        }
    }
    cycle = (cycle + 1) mod tcqf.cycles + 1
}
```

Additional explanatory text to reconfirm that “schedule to send” can be arbitrary time within the cycle, but that order of dequeuing needs to be maintained.

Any better way to describe this ?

# Changes from -01 (IETF115)

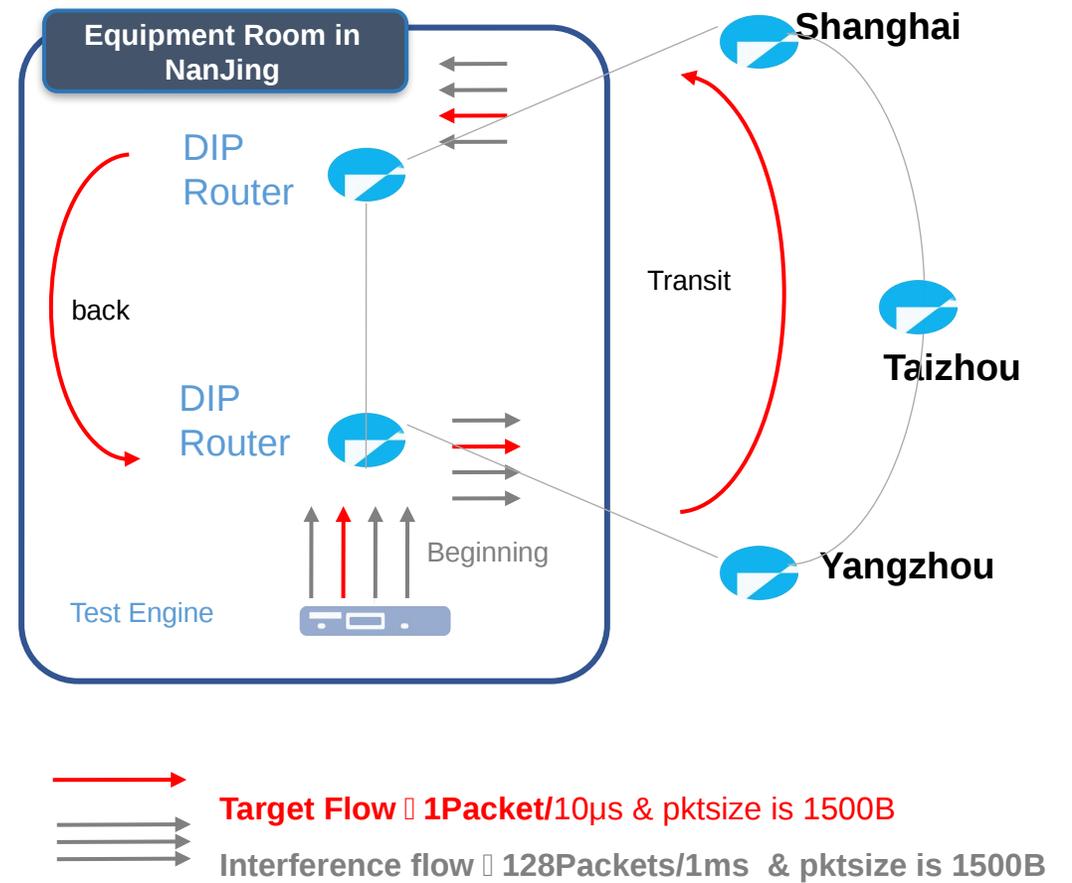
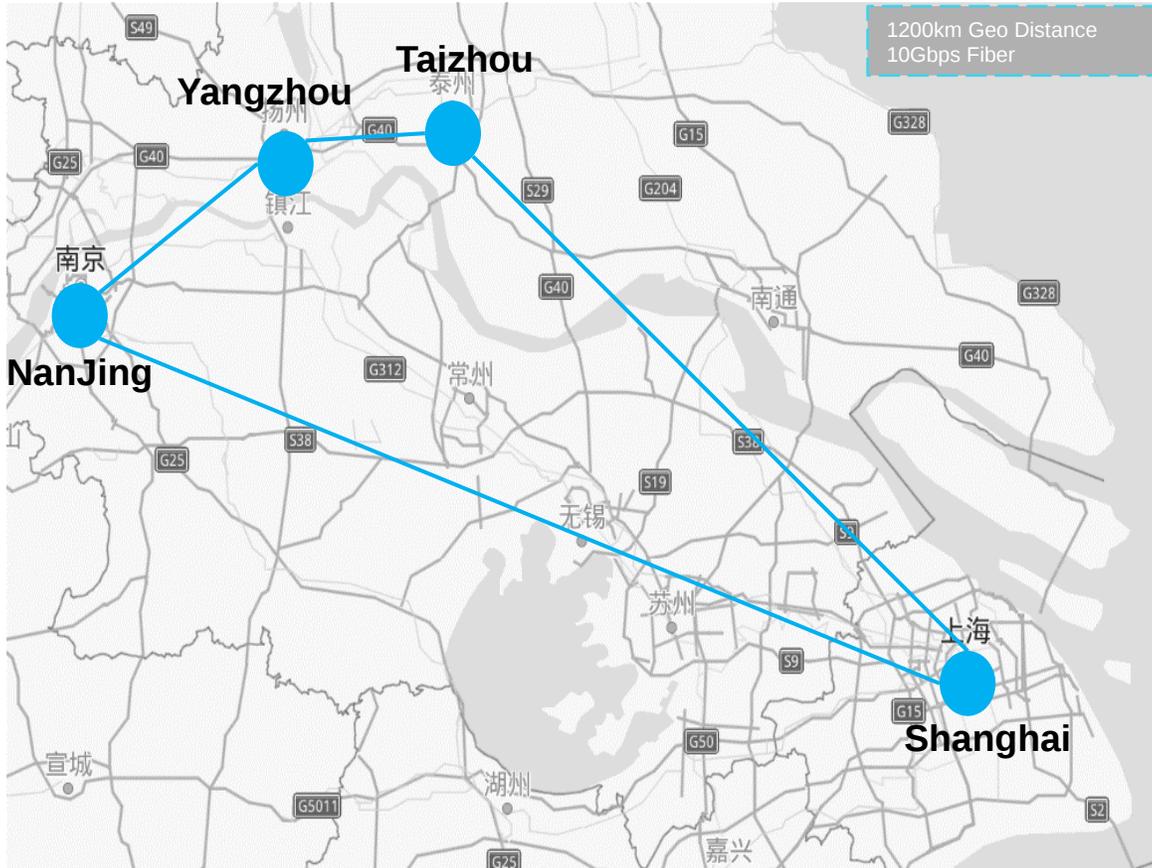
- Feedback from Lou Berger
- Added section “controller plane considerations”
- TCQF applicable with centralized control plane (AC / PCE)
  1. Simple AC policy (as outlined in ingres shaper): max number bits/flow in each cycle.
  2. More complex option (no spec for ingres shaper): allocate bits in fewer than ever cycle for flow (e.g.: could use gates as from TSN).
- TCQF applicable to distributed controller plane
  - Aka: RSVP(-TE) on-path/per flow admission control
  - Simple to make work with 1., not clear if/how to do 2.
  - Will eliminate per-flow-stateless benefit in control-plane  
But maintains per-flow-statelessness in high-speed HW-forwarding-plane!

# Changes from -01 (IETF115)

- Added reference/summary to CENI validation in 2020
  - Validation report alas chinese language
- CENI: Chinese research network
  - Across mayor chinese cities
- Used 100Gbps interfaces prototype WAN routers with TCQF (“DIP2”) in FPGA



# CENI TCQF (“DIP”) Testbed 2020



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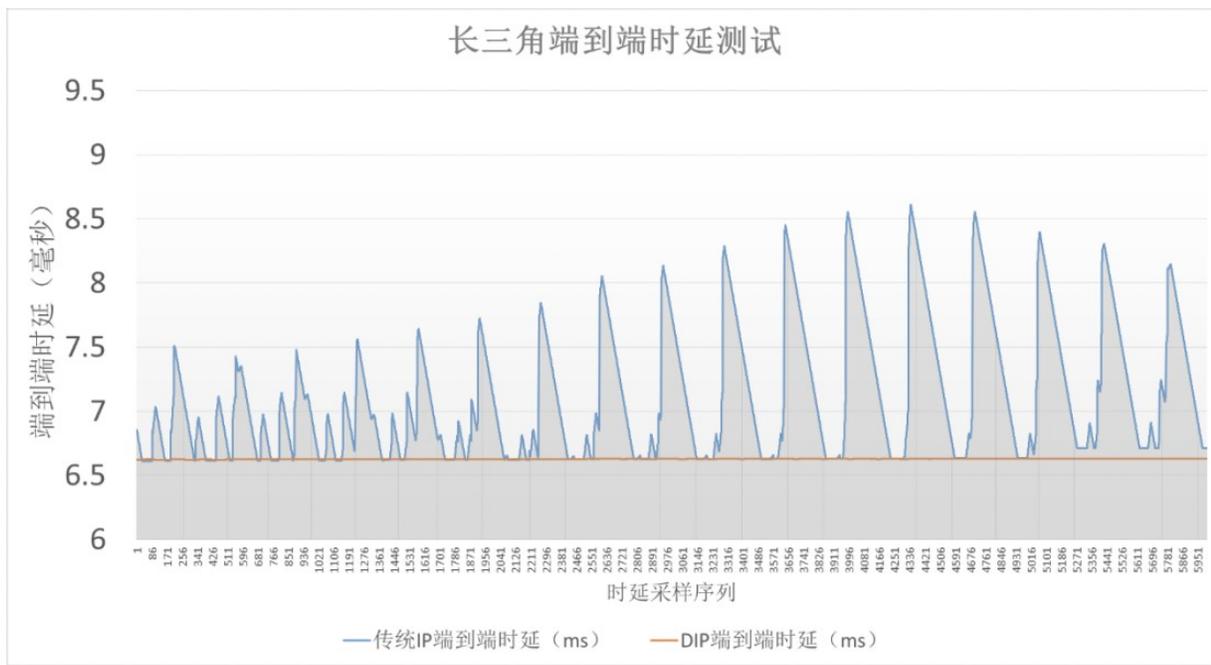


表 4 长三角综合试验网 DIP 测试统计结果

干扰流数量	传统 IP 转发端到端时延 (微秒)				DIP 转发端到端时延 (微秒)			
	最小	平均	最大	最大抖动	最小	平均	最大	最大抖动
1	6304	6306	6386	<b>83</b>	6360	6374	6389	<b>29</b>
2	6304	6311	6564	<b>261</b>	6360	6374	6389	<b>29</b>
3	6304	6321	6751	<b>447</b>	6360	6374	6389	<b>29</b>
4	6304	6370	7612	<b>1308</b>	6360	6374	6389	<b>29</b>
5	6304	6463	7977	<b>1673</b>	6360	6374	6389	<b>29</b>
6	6304	6577	8343	<b>2039</b>	6360	6374	6389	<b>29</b>
7	6304	6695	8608	<b>2304</b>	6360	6374	6389	<b>29</b>