

Jitter Reduction Mechanism for DetNet

draft-guo-detnet-jitter-reduction-mechanism-01

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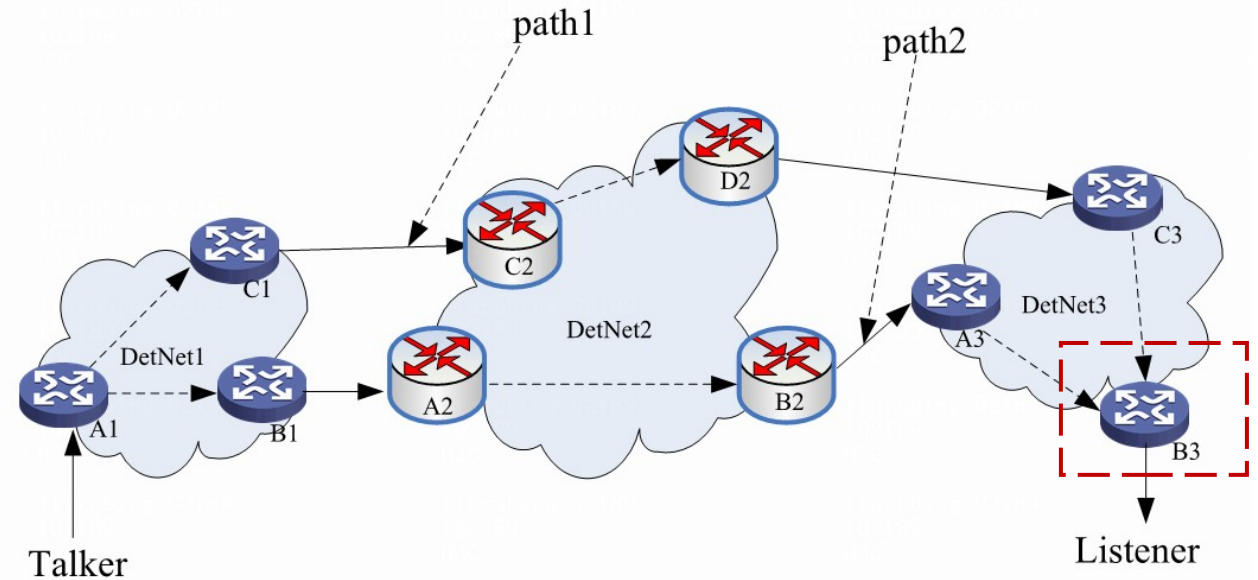
Draft work -00 to -01

- The draft has been modified in version 01:
 - Added descriptions on methods for residency delay processing.
 - Added descriptions how the solution contributes to enhancing network robustness.
- The following efforts and practices are being made :
 - Development of a solution to obtain reference delay.
 - Implementation of the solution into H3C's routers.

A Simple Instance

The overview of the solution is as follows:

- Collecting the transmission delay between the Talker and the Listener.
- Adding a reserved delay (selected from an engineering perspective based on deployment requirements) on the transmission delay of the longest path, referred to as the reference delay P_{thRefD} .
- Calculating the upper limit of compensation delay for each path.
- Collecting the actual transmission delay of the data packets during the transmission process, excluding the fixed and unchanged inter-domain transmission delay.
- At the COMPENSATION NODE, calculating the required compensation delay based on the actual transmission delay of the data packets and the upper limit of compensation delay.
- Performing the compensation at the COMPENSATION NODE.



B3 is COMPENSATION NODE

Why compensation at the last node

- Reducing jitter caused by various reasons

Enabling network deployers to flexibly choose different queuing mechanisms and network construction methods.

- Minimizing end-to-end latency

Each compensation requires a reference value, and compensation redundancy must be considered. When a data packet undergoes multiple rounds of delay compensation, it will increase the overall delay. Compensation should ideally only be performed once closing to the Listener.

- Achieving optimal results, minimizing costs and resource constraints

No matter where delay compensation takes place, there is always the possibility that multiple transmitted data to be queued, resulting in queuing delays that reduce the effectiveness of compensation. Compensating at the very edge of the network aims to provide a standardized approach to reduce end-to-end jitter, and to achieve the best results with the smallest cost.

Our Validation in Lab

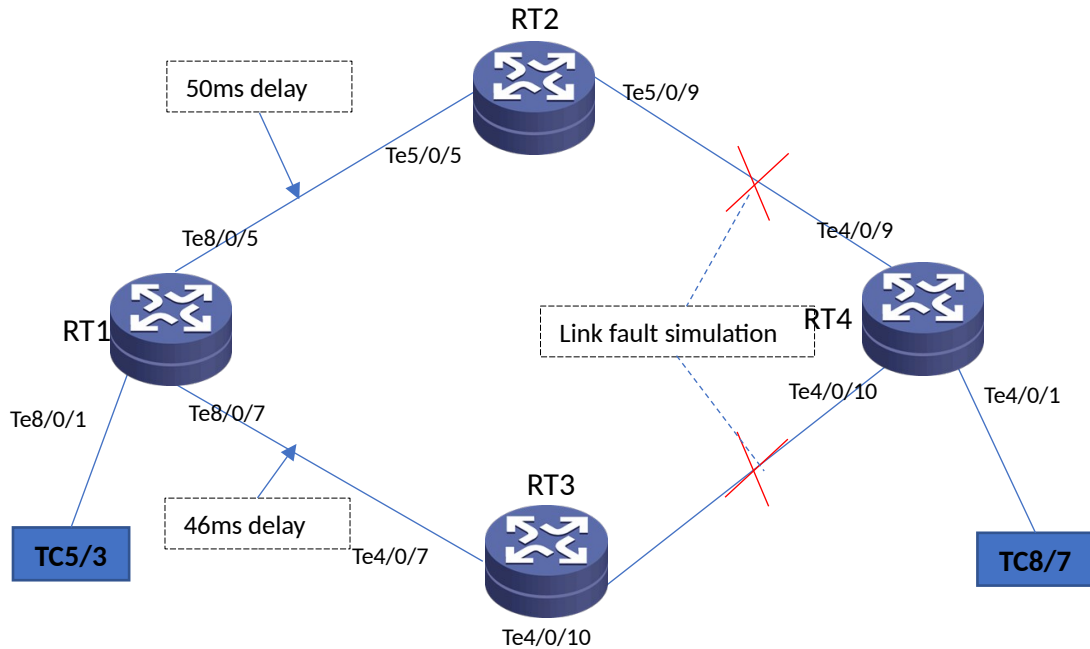


FIG. 1 Lab Network

Note for FIG.1

1. Imposing additional transmission delays of 50ms and 46ms on the two links respectively using Spirent Attero-100G.
2. RT1, RT2, RT3, RT4 are H3C's CR16K routers with 100G interfaces.
3. TC5/3 and TC8/7 are two ports of tester, acting as Talker and Listener.

Note for FIG.2

4. Column 1 holds the timestamps of receiving 4 pairs of OAM messages on the Tail Node, column 2 holds the corresponding sending timestamps on the Head Node, and column 3 holds the corresponding path delays.
5. The Max Path Delay is 50266852 ns.

Test setup:

6. Setting PthRefD as 51000000 ns
7. Constructing 50 DetNet flows with a total bandwidth of 1G bps and packet size of 1280 bytes.
8. Constructing 5000 background flows at 100G bps with random packet size from 64 to 9600 bytes.

Test Operation:

9. Performing alternate fault simulations on Path 1 and Path 2
10. Observe the jitter values on the tester with and without compensation.

Test Result:

11. All jitter values on the tester are less than 12us with compensation.
12. The maximum Observed jitter exceeds 2ms without compensation.

	Head Node ns	Tail Node(ns)	delay ns
path1	170174979	216422111	46247132
path2	170179219	220442071	50262852
path1	170324979	216572071	46247092
path2	170325219	220592071	50266852
path1	170325459	216572311	46246852
path2	170325699	220592311	50266612
path1	170325979	216572671	46246692
path2	170333499	220592551	50259052

FIG.2 Path latency data

Benefits

- It can be applied to either a single domain or multiple domains.
- Time synchronization is necessary only between the Ingress Gateway and the Egress Gateway within each DetNet domain, not all the nodes in a single DetNet domain.
- Time synchronization is only required within each synchronous domain, not between synchronous domains.
- The Ingress and Egress NODE collect the actual transmission delay in each domain.
- Compensate the transmission delay at the COMPENSATION NODE connected to the Listener.

Next step

- **Feedback / collaboration highly welcome!**

Thank you!

Backup-Reference Architecture

Virtual Clock Reference Plane (VCRP): Provides a time synchronization reference for the clock used for DetNet data plane [DDP] timing.

In some high-precision demand scenarios, the resident delay within the network domain may need to be adjusted.

VCRP provides a unified reference standard for adjustment, and the controller needs to participate in maintenance.

