Carrying SR Algorithm information in PCE-based Networks

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Motivation

• A PCE can compute SR-TE paths using SIDs with different Algorithms depending on the use-case, constraints, etc. While this information is available on the PCE, there is no method of conveying this information to the headend router.

• An operator may also want to constrain the path computed by the PCE to a specific SID Algorithm.

• SID Algorithm covers
  • SPF (Algo 0)
  • Strict SPF (Algo 1)
  • Flex-Algo (Algo 128-255)

• Computing path with a fewer SIDs
Draft summary

• SR-ERO and SRv6-ERO Subobject extension to carry SR Algorithm
• SR Algorithm constraint encoded in new TLV in LSPA object
  • Flexible Algorithm path computation
    • Based on constraints and metric type from Flexible Algorithm Definition
    • Alignment with Flexible Algorithm path computation in IGP
      • Tie-breaking logic for FAD selection
      • Topology pruning
      • Usage of Flex-algo ASLA specific link attributes
  • Path computation with SID filtering
• New metric types
  • Path Min Delay Metric
  • P2MP Path Min Delay Metric
Latest changes

• Version change - 03 -> 05

• Early IANA codepoint allocation done
  • SR capability flag – Bit 5 in SR-PCE-CAPABILITY TLV
  • SR-ERO flag – Bit 7 in SR-ERO Flag Field
  • SR Algorithm TLV – Type 66 in PCEP TLV Type Indicators
  • Path Min Delay Metric – Type 22 in METRIC Object T Field
  • P2MP Path Min Delay Metric – Type 23 in METRIC Object T Field

• SRv6 related IANA registries not created yet

• Reduced number of authors to 5
Next steps

• Any existing implementations?
• WGLC after allocating codepoints for SRv6 related PCEP extensions