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Updates to the IPv6 Multicast Addressing Architecture
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Abstract

This document updates the IPv6 multicast addressing architecture by defining the 17-20 reserved bits as generic flag bits. The document provides also some clarifications related to the use of these flag bits.

This document updates RFC 3956, RFC 3306, RFC 4607 and RFC 4291.

Requirements Language

The key words "MUST", "MUST NOT", "REQUIRED", "SHALL", "SHALL NOT", "SHOULD", "SHOULD NOT", "RECOMMENDED", "MAY", and "OPTIONAL" in this document are to be interpreted as described in RFC 2119 [RFC2119].

Status of this Memo

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1. Introduction

This document updates the IPv6 multicast addressing architecture [RFC4291] by defining the 17-20 reserved bits as generic flag bits (Section 2). The document provides also some clarifications related to the use of these flag bits (Section 3.1) and also about IANA assigned SSM blocks (Section 3.2).

This document updates [RFC3956], [RFC3306], [RFC4607] and [RFC4291].

2. Addressing Architecture Update

Bits 17-20 of a multicast address are defined in [RFC3956] and [RFC3306] as reserved bits. This document defines these bits as generic flag bits so that they apply to any multicast address. Figure 1 and Figure 2 show the updated structure of the addressing architecture. The first diagram shows the update of the base IPv6 addressing architecture, and the second shows the update of so-called Embedded-RP.

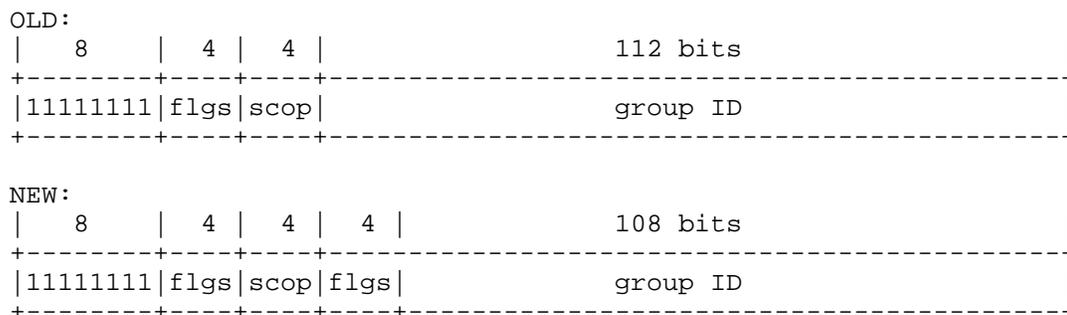


Figure 1: Updated IPv6 Multicast Addressing Architecture

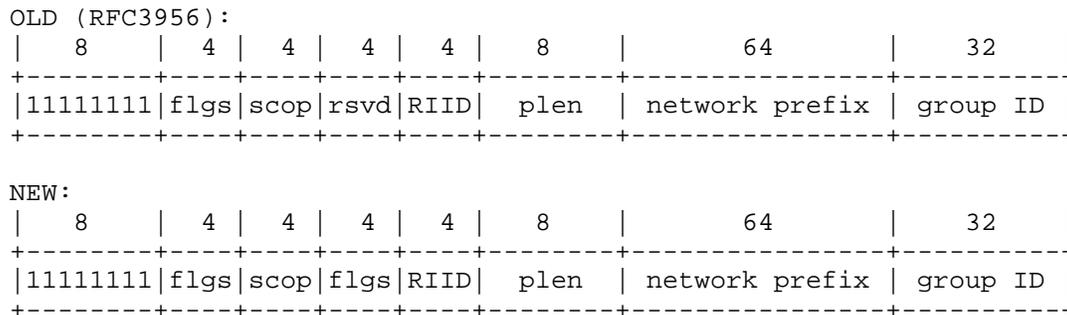


Figure 2: Embedded-RP with Updated IPv6 Multicast Address Arch.

Further specification documents may define a meaning for these flag bits. Defining the bits 17-20 as flags for all IPv6 multicast addresses allows addresses to be treated in a more uniform and generic way, and allows for these bits to be defined in the future for different purposes, irrespective of the specific type of multicast address.

3. Clarifications

3.1. Flag Bits

Some implementations and specification documents do not treat the flag bits as separate bits but tend to use their combined value as a 4-bit integer. This practice is a hurdle for assigning a meaning to the remaining flag bits. Below are listed some examples for illustration purposes:

- o the reading of [RFC4607] may lead to conclude that ff3x::/32 is the only allowed SSM IPv6 prefix block.
- o [RFC3956] states only ff70::/12 applies to Embedded-RP. Particularly, implementations should not treat the fff0::/12 range as Embedded-RP.

To avoid such confusion and to unambiguously associate a meaning with the remaining flags, the following recommendation is made

Implementations MUST treat flag bits as separate bits.

3.2. IANA Assigned SSM Block

Another issue related to SSM is the IANA assigned SSM address block. Per [RFC4607], ff3x::4000:0001 through ff3x::7fff:fff is the block for IANA assignments (<http://www.iana.org/assignments/ipv6-multicast-addresses/ipv6-multicast-addresses.xml>). However, IANA assignments are permanent addresses and should not have the transient bit set. Quoting from [RFC4607]:

"T = 1 indicates a non-permanently-assigned ("transient") multicast address."

4. IANA Considerations

This document may require IANA updates. However, at this point it is not clear exactly what these updates may be.

5. Security Considerations

Security considerations discussed in [RFC3956], [RFC3306], [RFC4607] and [RFC4291] MUST be taken into account.

6. Acknowledgements

Many thanks to B. Haberman for the discussions prior to the publication of this document.

7. Normative References

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