

# **YANG Data Model for IEEE 1588v2**

draft-jlx-tictoc-1588v2-yang-00

Yuanlong Jiang, [jiangyuanlong@huawei.com](mailto:jiangyuanlong@huawei.com)

Xian Liu, [lenc.liuxian@huawei.com](mailto:lenc.liuxian@huawei.com)

Jinchun Xu, [xujinchun@huawei.com](mailto:xujinchun@huawei.com)

# Backgrounds

---

- IEEE 1588v2
  - A critical sync technology in various application scenarios, widely deployed in the carrier networks;
  - 1588v2 MIB draft is progressing, but only with limited capability.
  
- YANG data model
  - Validation and rollback features;
  - Separation of configuration and state/statistics data ;
  - Support of multi-layer hierarchical data models ;
  - Reusable types and groupings ;
  - Formal constraints for configuration validation.

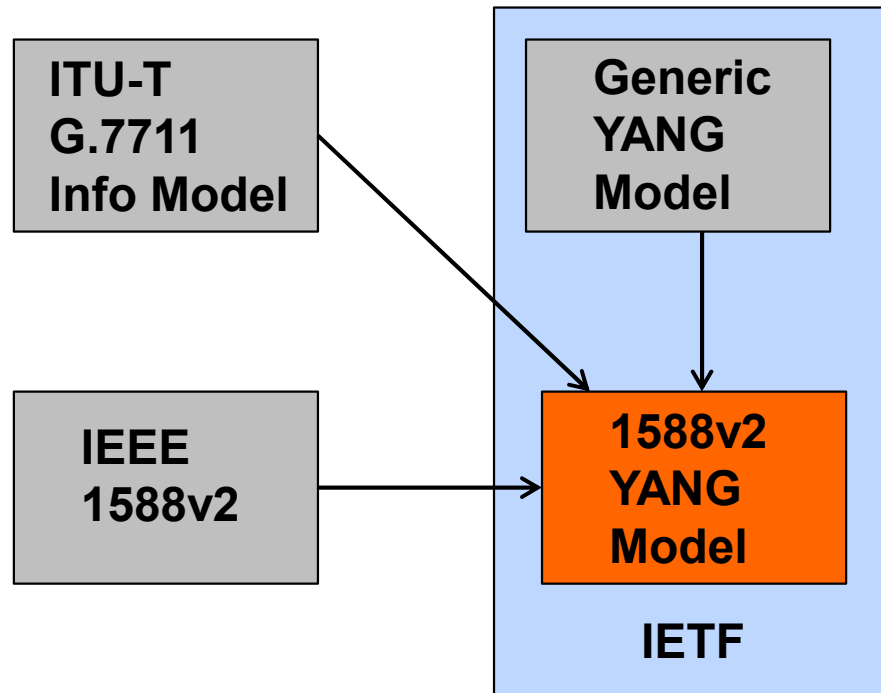
# Reqs & considerations

---

- Sync requirements
  - More configuration capability
  - Validation and fault management
    - Profiling of the current sync path
    - Fast diagnosis of a faulty path if sync is broken
- Compatible with 1588v2 MIB draft
  - State retrieval remains the same;
  - System info retrieval as it is;
  - Use YANG instead as the data modeling language

# Relationship with other SDOs

---



# ***YANG Hierarchy for 1588v2***

---

```
module: ietf-yang-ptp-query
  +--rw device-ptp-query-table
  | +--rw ptpDevicequery* [clock-identity domain-number]
  |   +--rw clock-identity      binary
  |   +--rw domain-number      uint32
  |   +--rw clock-current-DS
  |   +--rw clock-parent-DS
  |   +--rw clock-default-DS
  |   +--rw clock-running
  |   +--rw clock-time-properties-DS
  |   +--rw clock-trans-default-DS
  |     +--rw clock-identity?  binary
  |     +--rw num-of-ports?   uint32
  |     +--rw delay?          Enumeration
  |
  .....
```

# ***YANG Hierarchy for 1588v2***

---

```
module: ietf-yang-ptp-config
  +--rw ptpDeviceConf
  | +--rw ptpDevice* [deviceIdentity]
  +--rw todPortConf
  | +--rw todPort* [todPortIdentity]
  |   +--rw todPortIdentity      binary
  |   +--rw todDirection?       enumeration
  |   +--rw todProtocolType?    enumeration
  |   +--rw timeGradeMode?      boolean
  |   +--rw timeSource?         enumeration {connect-bits}?
  |   +--rw clock-source
  |   +.....
  +--rw ptpPortConf
  | +--rw ptpport* [ptpPortIdentity]
  |   +--rw ptpPortIdentity      binary
  |   +--rw portEnable?         boolean
  |   +--rw delayMechanism?     enumeration
  |   +.....
```

# *Next Step*

---

- Add more config capabilities in the next version
- Reviews and feedbacks from WG are greatly appreciated
- Welcome more people to join this work

---

*Thank You*