YANG Data Model for IEEE 1588v2

draft-jlx-tictoc-1588v2-yang-02

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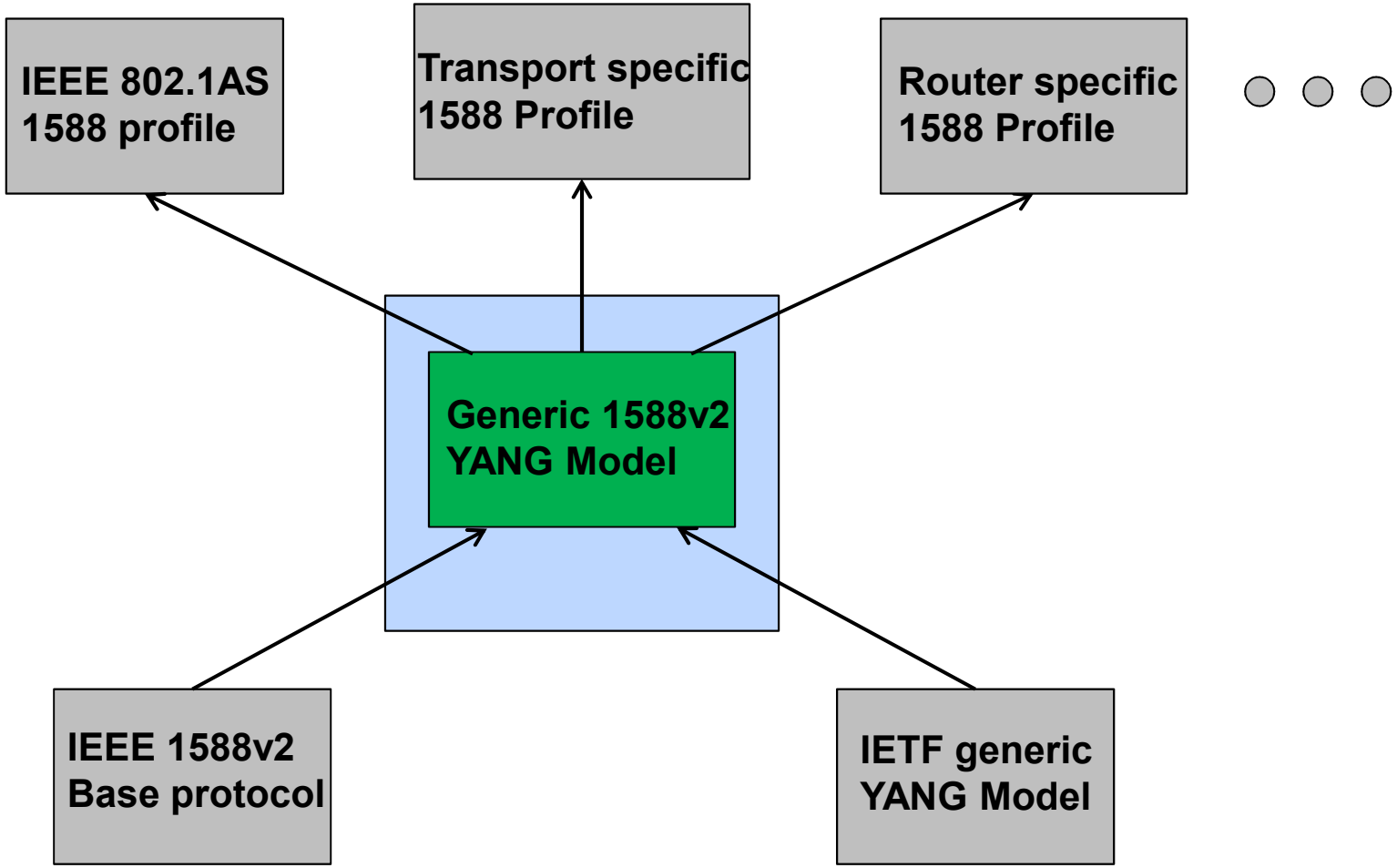
Backgrounds

- IEEE 1588v2
  - A critical sync technology in various application scenarios, widely deployed in the carrier networks;
  - 1588v2 MIB draft is progressing, but only with limited capability;
  - A more flexible 1588 model is needed to innovate the synchronization networks.
- YANG data model
  - Validation and rollback features;
  - Separation of configuration and state/statistics data;
  - Support of multi-layer hierarchical data models;
  - Reusable types and groupings;
  - Formal constraints for configuration validation.

Summary of Changes

- Router specific contents are split off
- RPC statements are removed
- Container names and leaf names are more closely matched with IEEE 1588v2
- Place all data sets in a "list", with a "key" of "domain-number"
  - the data sets of each clock are totally independent for each domain
- The port-DS data set and transparent-clock-port-DS are modeled as lists
  - Each clock contains at least one port, but can contain more than one port (i.e. BC or TC)

Relationship with other SDOs



YANG Hierarchy for 1588v2

```
module: ietf-yang-ptp-dataset
    +--rw ptp-datasets* [domain-number]
       +--rw domain-number   uint8
       +--rw default-DS
       +--rw current-DS
       +--rw parent-DS
       +--rw time-properties-DS
       +--rw port-DS-list* [port-number]
       +--rw transparent-clock-default-DS
       +--rw transparent-clock-port-DS-list* [port-number]
……
```

Next Step

- Reviews and feedbacks from the WG are greatly appreciated
- Progress this work jointly with IEEE P1588 SG

Thank You