

Data-Intensive Function Acceleration

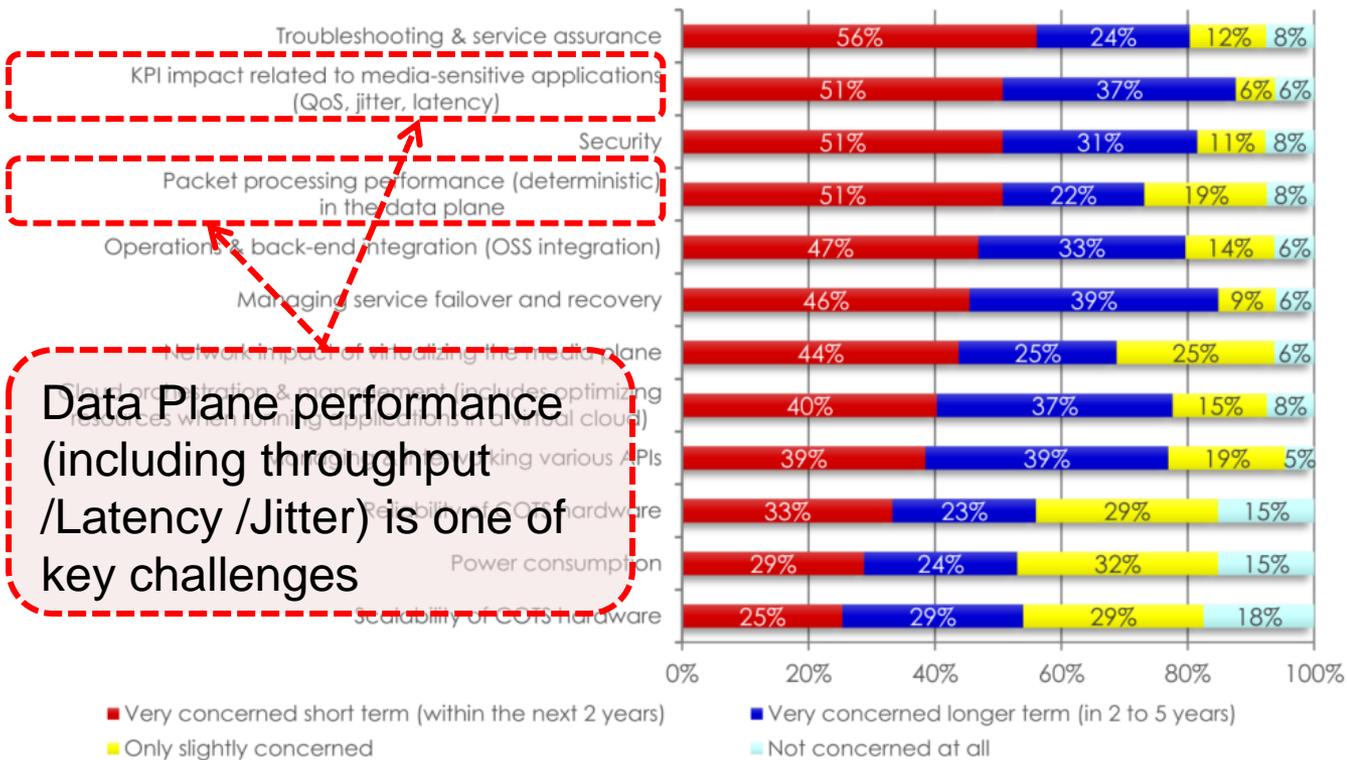
Jinwei Xia (xiajinwei@huawei.com)
Lu Huang (huanglu@chinamobile.com)
Ariel Gu (gurong_cmcc@outlook.com)

IRTF nfvrg, March 2017, Chicago.

Motivation

Figure 5: NFV Implementation Challenges

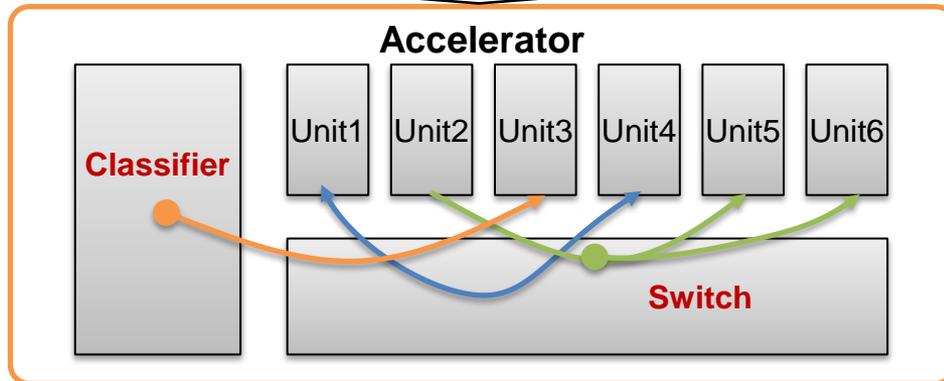
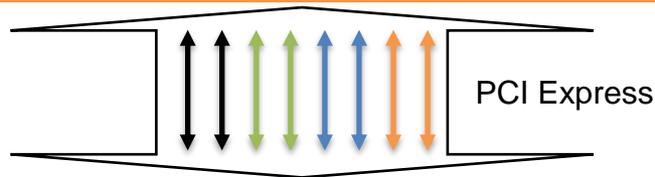
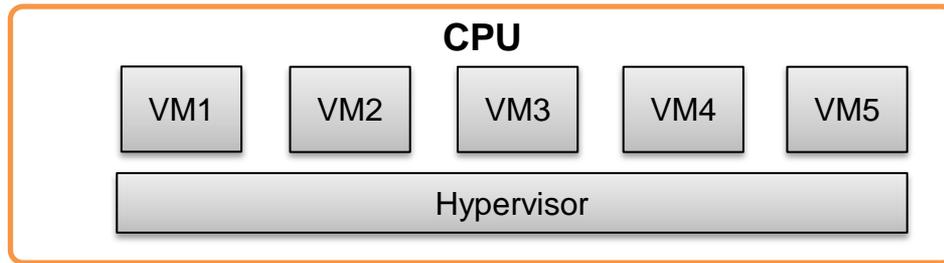
How concerned is your company about the following technical challenges related to NFV? (n=66)



Source: Heavy Reading NFV Multi-Client Study Q1 2014

- It's challenging to have low-latency and high-performance VNFs in NFV environment.

CPU + Accelerator



Benefits of X86

- Flexibility, Rapid Innovation
- Faster TTM

Benefits of accelerator

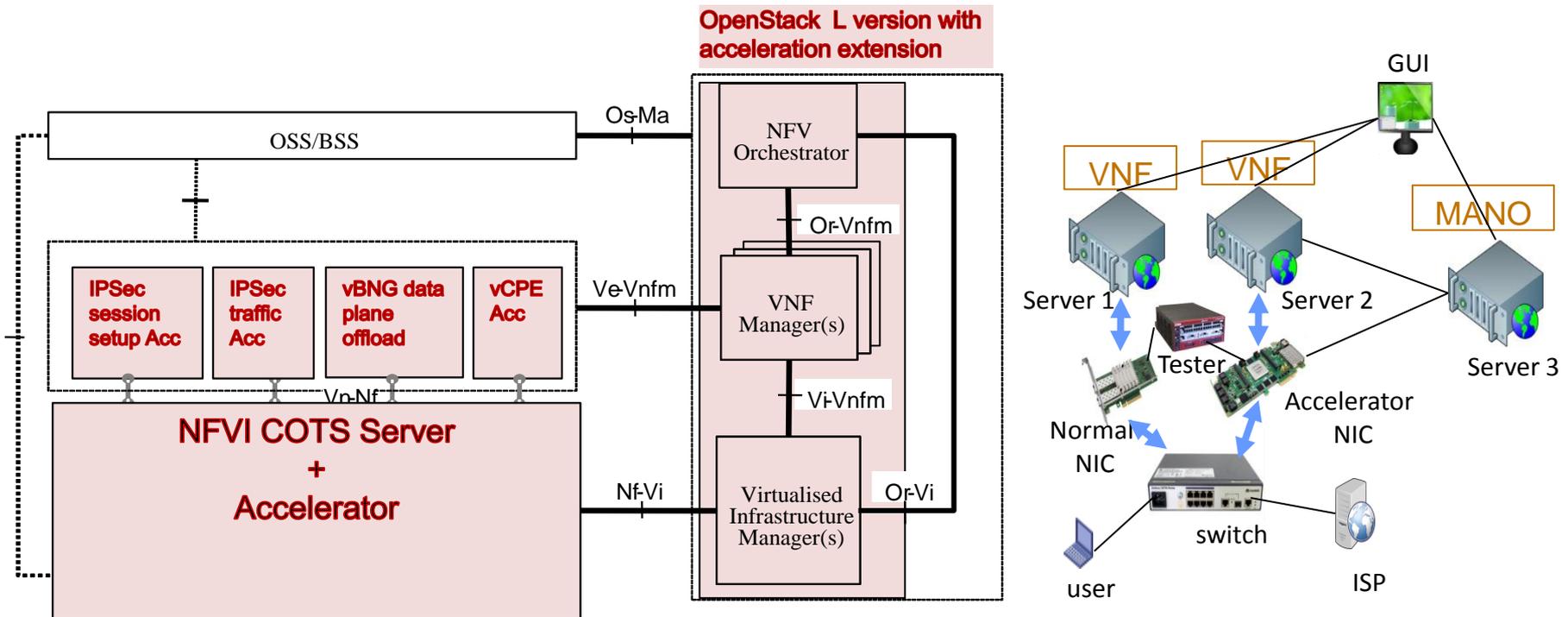
- improve throughput on small packet.
- decrease latency/Jitter
- save I/O cycles on X86
- classify incoming traffic, forward, load-balance and chain flows across VMs
- accelerate overlay networking, e.g. VxLAN, NVGRE
- accelerate packet processing, e.g. virtualized L2, L3, NAT

🌐 This should be a way to unite the flexibility of X86 and performance of accelerator.

Standard work in ETSI NFV IFA WG

- Acceleration Interface (IFA018) specifies the interface between data-intensive VNF and accelerator.
 - The interface allows the VNF to offload its data plane processing to the accelerator while keeping its control plane on the VM.
 - VNF instructs accelerator to process packets based on the rules in match-action tables via the following 3 sub-interfaces.
 - Control interface: add/update/query/delete the entries of the forwarding tables. Each entry includes the items such as forwarding table ID, forwarding table name, entry ID, match, action and etc;
 - Operation interface: report statistics and events to the VNF;
 - Packet I/O interface: forward non-accelerated packets and unmatched packets to the VNF;

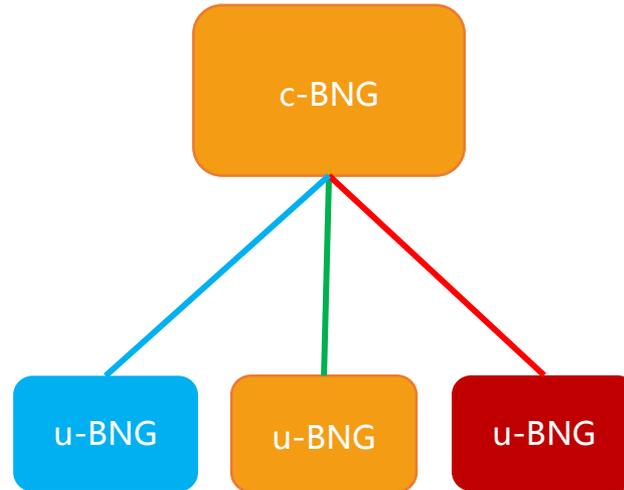
Acceleration PoC



- Acceleration PoC: Data-intensive Function Acceleration

- Use Cases: IPsec session setup Acc, IPsec traffic Acc, vBNG data plane offload, vCPE (OVS+NSH) offload.
- Timelines: starts from March 2017, aims to be demonstrated at SDN NFV Congress, The Hague, Netherlands, Oct 2017.

Relevant works in IETF NFV RG



- **draft-gu-nfvrg-cloud-bng-architecture-00**
 - Defines the architecture of cloud-based BNG devices with centralized control plane (CP) and user plane (UP) separation;
 - Similar to vBNG data plane offload use case in the Acceleration PoC if u-BNG is running on the accelerator;
- **draft-huang-nvo3-vxlan-extension-for-vbras-00**
 - Describes the VxLAN extension requirements for signaling exchanges between control plane and user plane of virtual BRAS;
- **need more auxiliary drafts**
 - Problem Statements I-D; Gap Analysis I-D; Requirements I-D; etc;

Make Sense?

More Question?