P4DNS: In-Network DNS

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Introduction

- Networks continue to increase bandwidths without achieving much latency reduction.
- Latency is particularly important in data center networks.
- In-network computing brings network computation closer to its use.
- We develop P4DNS using P4 → NetFPGA
  - 52x throughput improvement and 100x latency reduction over NSD
  - Identify areas where P4 is ill-suited for developing traditional applications on an FPGA.
Architecture

Data Plane (P4) + Control Plane (Python)
Design Lessons: Hardware for Traditional Protocols

- Control plane is a bottleneck:
  - Protocols with mutable state tax this bottleneck.
- Existing protocols are designed for software:
  - DNS uses C-style strings.
    - String length is not clear until you have reached the last character.
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But, partial implementations can work:
- P4DNS achieves 52x throughput improvement and 100x latency improvement.
P4 on Hardware Limitations

- Field length limitations: 384 bits.
- Complex parsing state machines used excessive hardware resources on FPGAs.
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- For many applications, a simple bitstream is enough.
- FPGAs remove some advantages (recursion) of state machines.
Conclusion

- We implemented P4DNS, a DNS accelerator integrated into a P4 switch using P4→NetFPGA.
- We demonstrated potential for large performance improvement without changing existing protocols.
- But P4 is not without limitations for hardware targets.